

Practical Current Feedback Amplifier Design Considerations

The current-feedback (CMF) amplifier is a fundamentally different approach to high-frequency gain blocks. Not just an input stage, it is a full amplifier topology. It has outstanding characteristics in several areas: very high slewrates, -3dB bandwidth which is almost constant with increasing circuit gain, and low high-frequency distortion. Almost all commercial CMF products offer these benefits, but, sadly they also exhibit limitations that are seldom publicized. This article is intended to point out the theoretical basis for the CMF amplifier's strengths and weaknesses, and some ways of coping with its problems.

Figure 1 shows the modern fundamental CMF circuit, with feedback applied through R_F to implement an operational voltage follower. Q1 through Q4 form a complementary buffer. The terminal called -Input is thus actually an output, a buffered replica of the voltage at +Input. Q3 and Q4 idle at a quiescent current proportional to the geometric mean of I_1 and I_2 and a scale factor dependent on the relative sizes of Q1 through Q4. When the feedback loop is at null, no error current will flow to the -Input, and Q3 and Q4 draw equal collector currents (we will ignore base current errors in this discussion). Q3's collector current is mirrored by Q8 and Q9 and delivered to the gain node. Q4's collector current is mirrored by Q5 and Q6 and sent to the gain node to balance against the previous mirrored current. Transistors Q11

through Q14 buffer the voltage at the gain node and present it as the output voltage.

To understand the behavior of the circuit, imagine that the +Input and the output had been resting at zero volts and a one-volt positive step is delivered to the +Input. The input buffer Q1 through Q4 will very quickly replicate the step at the -Input terminal and the step voltage is thus impressed upon the feedback resistor R_F , since the output has not yet had time to move. Let us assume that R_F is $1k\Omega$, a typical value. The one-volt step then will cause a transient one milliampere current to flow through R_F , increasing Q3's current by $500\mu A$ and decreasing Q4's current by $500\mu A$. Q9's collector current will then increase by $500\mu A$ and Q6's collector current will decrease by $500\mu A$, assuming the current mirrors have a gain of one. The milliampere of transient error current through R_F thus is transferred to the gain node of the amplifier and serves to slew the node positive, at a rate determined by C_{COMP} . The output, following the gain node, will move positive until equilibrium is reached where no current flows through R_F and currents to the gain node balance.

Slewrate

The output slewrate is the feedback current divided by C_{COMP} . if the input step were increased to two volts, twice the previous error current would flow through R_F and twice

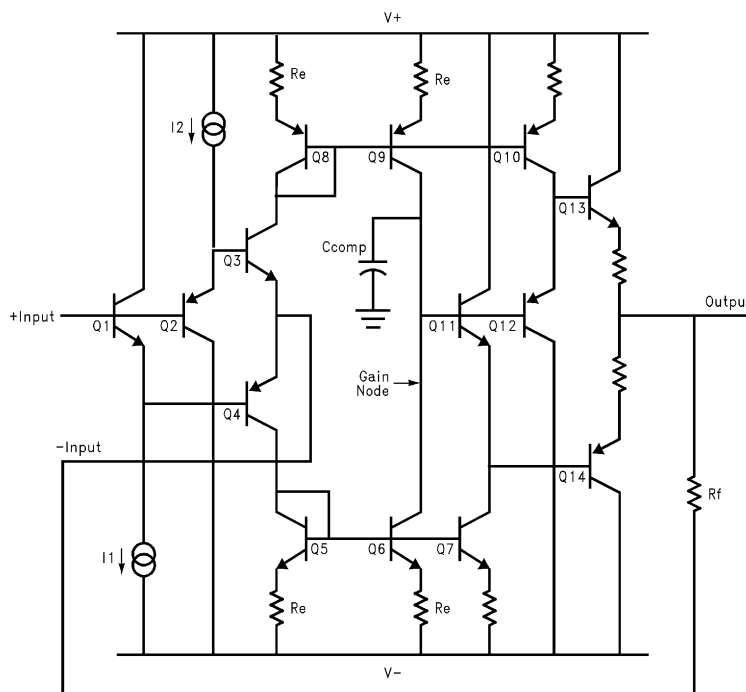


FIGURE 1. A TYPICAL CURRENT-FEEDBACK AMPLIFIER CONNECTED AS A UNITY-GAIN FOLLOWER

the slew current delivered to C_{COMP} , yielding twice the previous slewwrate. Even if the error current through R_F exceeded the quiescent idle currents through Q3 and Q4, one of the two transistors would simply turn off and all error current would be delivered through the other transistor and associated current mirror in class A-B operation. In essence there is no slewwrate limit in the conceptual CMF amplifier, and all step inputs produce the ideal single-pole exponential output response.

The high-frequency advantages of the CMF topology are manifold. The absence of slew limitation yields low distortion for large and high-frequency signals, even up to the normal small-signal bandwidth limitation. Since slew current is produced by the feedback error signal, the idle currents can be low without seriously affecting slewwrate. And as we will see, the bandwidth is determined mainly by R_F and C_{COMP} and does not diminish rapidly with increasing closed-loop gain.

As in all circuits, there are limitations. We will consider time domain aberrations first. For increasingly large input steps and slewwrates, the error current through R_F also increases. A fast 10V input step could produce a 10mA peak error current, and this would not be supportable in many amplifiers. Typically, transistors in the current mirrors would saturate during the transient, causing slew and settling aberrations. Monolithic amplifiers support 500V/ μ s to 2000V/ μ s slewwrates, but many devices display full-out step response that is "out of control". Saturation also occurs more readily at high temperatures, and takes longer to settle out, so amplifiers that seem to not exhibit saturation distortions at room temperature often do when hot.

The other slew distortion mechanism is input stage slew limitations. Q1 has an essentially unlimited positive slew capability, but its negative-going slewwrate is limited by I1 and parasitic capacitance at Q1's emitter. Q2 similarly is not restricted in its negative-going slewwrate, but I2 limits its positive slewwrate. The result is that the replicated voltage presented at -Input is limited in each direction of slew by the respective current-source and parasitic capacitance. The maximum input slewwrate might be less than the output slewwrate (the slew allowed by the supportable error current from R_F mirrored to C_{COMP}), or it may be more. If the input slewwrate is less than the output slewwrate, -Input will "float" toward the new +Input voltage and the output will follow that slew-limited response.

Some CMF amplifier designs are simply not recommended for positive gain connections. These amplifiers are to be connected in inverting gain mode so that the +Input does not see signals at all. Their +Input is not a high impedance and does not offer good input slewwrate.

This is the ultimate workaround to input stage limitations: connect the amplifier as an inverter.

This runs counter to most instrument designs, and as we will see, can often be inconvenient in many other ways.

Fortunately, there are many CMF amplifier products designed to work well in the non-inverting mode.

Settling Behavior

With their large slewwrates, one would expect the CMF amplifier to settle very quickly to high accuracies. This is only partly true; the CMF amplifier can settle very fast to moderate accuracies but displays large thermal settling tails. To see why this is true, consider the offset voltage between -Input and +Input. There is the difference of $V_{be}(PNP) - V_{be}(NPN)$ at -Input relative to +Input. If we raise +Input by one volt, Q1 will dissipate less power since its V_{CE} was reduced, and $V_{be}(NPN)$ will increase slightly as the transistor cools. Conversely, Q4 will gain a volt in V_{CE} , so its $V_{be}(PNP)$ reduces as it warms. Unfortunately, the drift in V_{be} 's do not cancel. Note that these are device thermals; the device dissipates power just under its emitter in the collector region. The heat source is so physically small that it spreads and diminishes in a space smaller than the overall size of a transistor, and no device-to-device thermal coupling can be employed in an integrated layout to remove the effect.

To get an idea of the magnitude of the thermal settling errors, let us assume all transistors run at quiescent currents of 1mA and that each device has a 70°C/W thermal coefficient. Each transistor changes dissipation by 1mW, causing a 0.07°C temperature change. Since a silicon junction voltage changes by 1.7mV/°C each device V_{be} changes 120 μ V, for a total thermal error of 240 μ V per volt of input. This 0.024% thermal error eliminates any concept of 0.01% settling, at least in positive-gain connections, and most CMF amplifiers are specified for 0.1% settling times instead. Figure 2 shows the settling response for an EL2020 to a 10V step in unity-gain connection. It settles very quickly to 0.1% bounds, 70ns for a 10V step, but has a thermal input tail that pushes 0.01% settling much longer out.

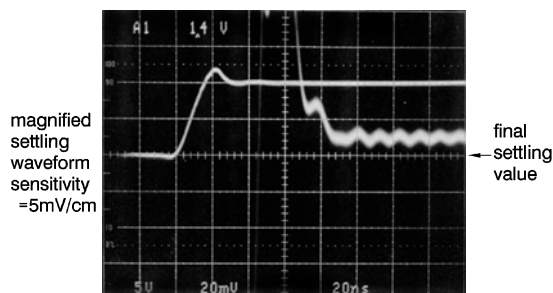


FIGURE 2. SHORT-TERM SETTLING CHARACTERISTIC OF EL2020 (UNITY GAIN MODE)

Further settling aberrations can be generated as feedback current errors into the -Input terminal. The current errors are multiplied by R_F to contribute an output voltage error. Assuming the current mirrors have a unity gain, any current variation into the gain node has a direct contribution to the feedback error current. The main source of error current, as far as settling is concerned, is thermal error within the

current mirrors. There are two popular topologies of CMF design where in one case the current mirrors add little to feedback current errors and in the other case their effect dominates all other settling errors. The simple two-transistor current mirrors Q5/Q6 and Q8/Q9 shown in Figure 3 is an example of the error-prone kind.

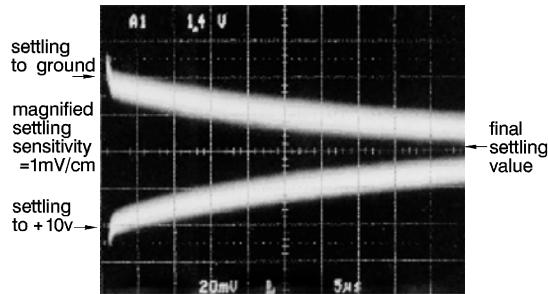


FIGURE 3. LONG-TERM SETTLING TAIL OF EL2020 (UNITY GAIN MODE)

Let us assume that $R_F = 1k\Omega$ and $R_e = 300\Omega$. Assume the gain node and output voltage move by one volt in response to a signal. Further assume that Q6 and Q9 have 1mA quiescent current and have a $70^\circ\text{C}/\text{W}$ thermal coefficient. As in the previous thermal calculation, the volt of V_{ce} change across the transistors will cause a 0.07°C temperature change in the device, for a V_{be} change of $120\mu\text{V}$. The diode-connected transistors Q5 and Q8 do not share in this temperature change, so the V_{be} change, divided by $R_e = 300\Omega$, creates a $0.4\mu\text{A}$ error into the gain node.

This error is doubled and reflected as a current error into -Input. The $0.8\mu\text{A}$ error, multiplied by $R_F = 1k\Omega$, yields an additional 0.08% thermal settling error.

This simple current mirror offers the widest bandwidth, greatest high-frequency linearity, most docile behavior for its bandwidth, and transient current capability, but much worse thermal errors than the more common Wilson type. Generally, CMF amplifiers whose transimpedance is greater than $150k\Omega$ have Wilson mirrors.

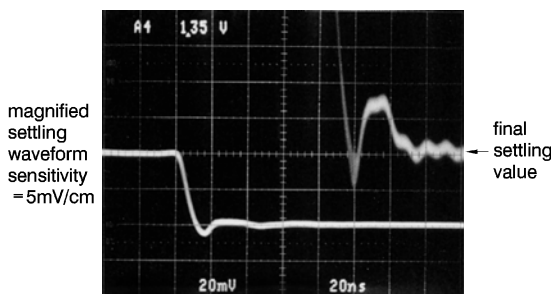


FIGURE 4. SHORT-TERM SETTLING CHARACTERISTIC OF EL2020 (INVERTING GAIN OF -1)

Figure 4 shows the settling response of the EL2020 connected in inverting mode ($A_V = -1$). Because the input stage does not have to move with the signal, it does not add thermal error and only -Input error current limits settling

quality. Although the 0.1% settling time is slowed to about 100ns, the amplifier can now settle to 0.01% in 130ns. As the figure shows, the settling tail reduced from the 0.024% size of Figure 2 to 0.007% in this connection.

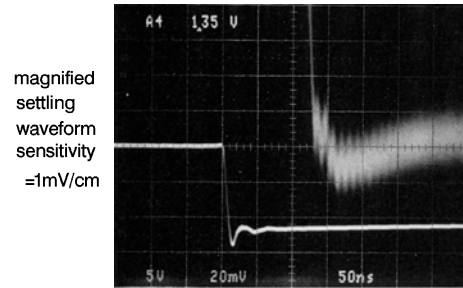


FIGURE 5. MAGNIFIED SHORT-TERM SETTLING CHARACTERISTIC OF EL2020 (INVERTING GAIN OF -1)

In any event, the CMF amplifier is still prone to load-driving thermal feedback effects. The input and current mirror stages are very hard to place on an IC so as to completely reject temperature changes on the die emanating from the output transistors. In general, if quality settling or best DC accuracy is desired, the CMF amplifier should be loaded as lightly as possible. 50Ω or 75Ω systems are poor choices for moving quality settling signals; direct device-to-device connection is best to avoid load-induced thermals.

Ultimately, the CMF is not the best choice for very high-accuracy settling, although it excels in the 8–10-bit realm. At 12-bit accuracy and above, properly designed traditional voltage feedback amplifiers dominate.

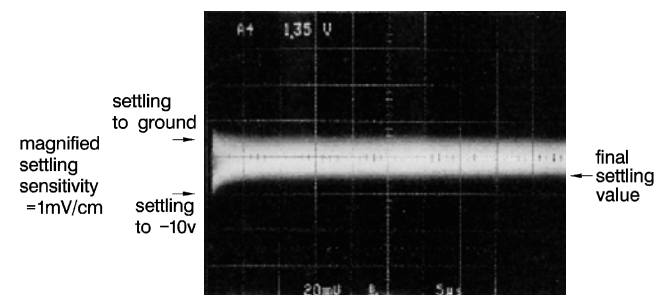


FIGURE 6. LONG-TERM SETTLING TAIL OF EL2020 (INVERTING GAIN OF -1)

Gain Accuracy

Figure 7 shows the small-signal macro-model of a CMF, used in positive-gain connection. The input buffer presents a copy of the +Input to the -Input terminal, but has an output impedance of R_{IN-} . The dotted line emanating from the side of the input buffer represents a connection to a current source whose value is a copy of the current flowing into -Input. This current is applied to the gain node, which is loaded at DC by R_{OL} and over frequency by C_{COMP} , the compensation capacitor. The external gain-setting resistors

are the previous R_F and an added R_G . Finally, C_{IN-} is the external parasitic capacitance at the -Input terminal.

The ideal gain of the fed-back amplifier is:

$$\frac{V_O}{V_{IN}} = \frac{R_F + R_G}{R_G}$$

which we will term A_0 .

The precise expression for the fed-back gain is

$$\frac{V_O}{V_{IN}} = A_0 * \frac{1}{1 + \frac{R_F + A_0 * R_-}{R_{OL}}}$$

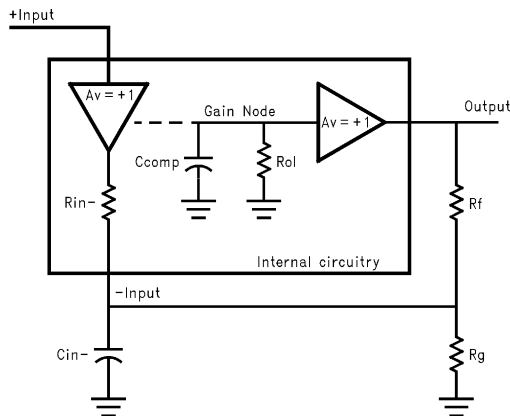


FIGURE 7. SMALL-SIGNAL EQUIVALENT CIRCUIT OF THE CURRENT-FEEDBACK AMPLIFIER

The added term is near unity since R_{OL} is a large number. This term is the gain accuracy expression as a function of amplifier characteristics and feedback resistors. The gain error can be approximated as:

$$\text{Gain Error} = \frac{R_F + A_0 * R_-}{R_{OL}}$$

There is no occurrence in the equations of A_{VOL} , the open-loop gain of the CMF amplifier. Actually, A_{VOL} is an "imaginary" parameter which is a holdover from voltage-feedback days and has no meaning with respect to the CMF amplifier. Unfortunately, few data sheets offer R_- . R_- can be estimated as:

$$R_- = \frac{R_{OL}}{A_{VOL}}$$

This is mathematically exact, but the typical R_{OL} and A_{VOL} numbers offered in data sheets may not give precise estimates of R_- . For CMF amplifiers drawing supply currents around 16mA, R_- ranges from 10Ω to 25Ω; for lower currents around 8mA, R_- typically increases to 50Ω. Using $R_{OL} = 1M\Omega$, $R_- = 50\Omega$, and $R_F = 1k\Omega$, the gain error is 0.105% for unity fed-back gain and increases rapidly beyond a gain of 20. This is a key consideration in the CMF amplifier: gain

accuracy is seldom as good as in most voltage-feedback amplifiers.

Furthermore, gain accuracy reduces with heavy output loading since the output buffer reflects the load as a reduction in R_{OL} . The CMF is seldom used for closed-loop gains of more than 50, since amplifier gain and the value of R_G become too small to retain gain accuracy.

On the other hand, the gain accuracy did not reduce appreciably between the closed-loop gains of 1 and 10. This gain range is the "sweet range" of CMF amplifiers. Note that this relatively limited gain accuracy does not suggest a non-linear situation; the CMF is much more linear open-loop than voltage-feedback amplifiers and does not rely on massive voltage gain to be linear in feedback.

This discussion of gain accuracy was based on open-loop gain; there are three subtle aberrations that make this value optimistic. The first effect is the input common-mode rejection ratio, or CMRR. This effect places an offset on -Input proportional to the signal level on the +Input terminal. The offset is indistinguishable from an input signal, and in non-inverting gain configuration creates a gain error. The typical CMRR for the CMF amplifier is 50dB to 60dB, so that gain error can be as poor as 0.3%.

The second gain error is due to voltage sensitivity in the -Input terminal's bias current. As the +Input terminal voltage moves with signal, early errors between Q3 and Q4 modulate their alphas and thus mismatch their quiescent collector currents. The mismatch in currents must be made up for as -Input bias current variation. The term for this effect is -ICMR. A -ICMR error, multiplied by R_F , creates an output error similar to CMRR errors. -ICMR quantities range from 0.2μA/V to 10μA/V. In our CMF amplifier example -ICMR would be around 1μA/V. Using a 1kΩ feedback resistor would create an output error of 1mV/V, indistinguishable from a 60dB CMRR input error in unity gain connection. The -ICMR error is an output error, and reduces in input effect as the overall fed-back gain is increased. For instance, a gain of +10 causes -ICMR errors to be ten times less significant.

The third such error source is the thermal settling error previously discussed. At frequencies below 1kHz, the settling error is indistinguishable from CMRR or open-loop gain limitations. At frequencies above 100kHz, however, thermal time responses are too slow to make appreciable errors, and gain accuracy can actually improve. The amplifiers will show a small drop in gain below these frequencies and a small increase in gain above. The variation in gain is about the same magnitude as the settling tail. Thus, the better-settling CMF amplifiers will show thermal errors too small to affect overall gain accuracy over (low) frequency, while the poorest-settling amplifiers can display as much as a 0.2% gain bump in mid-band frequencies.

Frequency Response

For the best gain accuracy, therefore, the inverting connection should be used. Ideal frequency response is calculated by inserting C_{COMP} in parallel with R_{OL} :

$$\frac{V_O}{V_{IN}} = A_0 * \frac{R_{OL}}{(R_{OL} + R_F + A_0 * R_-) + s C_{COMP} R_{OL} (R_F + A_0 * R_-)}$$

The -3dB bandwidth of this expression occurs at a frequency of:

$$F_0 = \frac{1}{2\pi C_{COMP} (R_F + A_0 * R_-)} * \frac{R_{OL} + R_F + A_0 * R_-}{R_{OL}}$$

The term on the right is quite close to unity for any CMF application and will be ignored. Since $A_0 * R_-$ is usually much less than R_F , R_F dominates the expression for bandwidth over a wide range of closed-loop gain. This gives a bandwidth relatively independent of gain (or R_G), a major advantage for the CMF amplifier. The bandwidth falls to 1/2 of maximum when the gain is equal to R_F/R_- , or 20 in our example.

This first-order analysis ignores the effect of C_{IN-} and is an expression of what we will refer to as the “natural bandwidth” of the CMF amplifier. We will use the term natural instead of dominant pole because the pole is not completely dominant in every CMF design. The effect of C_{IN-} is to insert a secondary pole in the frequency response of the circuit. This secondary pole usually coincides with the output resonance of both the input and the output buffers, and the overall frequency response is further complicated by phase delays in the current mirrors.

Figure 8 is a simulation of the frequency response of the idealized circuit of Figure 7 at unity gain with a variety of C_{IN-} values, for a C_{COMP} of 3pF. With a C_{IN-} of zero, the frequency response is single-pole in nature and the -3dB bandwidth coincides with the “natural bandwidth”. With increasing C_{IN-} , a high-frequency zero is introduced which tends to maintain gain over frequency. At a gain of +1, the zero caused by $C_{IN-} = C_{COMP}$ would potentially cancel the pole caused by C_{COMP} itself. Unfortunately, nature is not so generous and this is an unattainable trick.

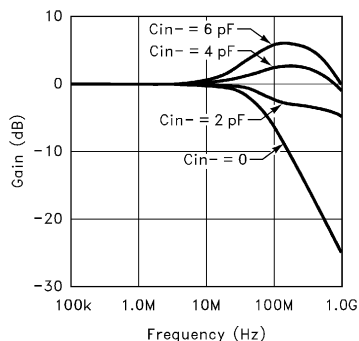


FIGURE 8. IDEAL CMF RESPONSE WITH VARIOUS VALUES OF C_{IN-}

Figure 9 shows the effect of C_{IN-} on a realistic CMF model. The current mirrors and output stage were modeled as having 200MHz single-pole bandwidths each, a realistic value in our example where the natural bandwidth is 50MHz. The limited bandwidths of the mirrors and output stage cause C_{IN-} to produce different aberrations. C_{IN-} still causes the bandwidth to expand, but at the expense of peaking. Peaking causes undesirable ringing in transient responses, and about 2dB of peaking is generally a gracious maximum. Only about 2.5pF of C_{IN-} can be tolerated for 2dB of peaking in our example, and this is a practical value. However, R_F and R_G must be connected directly to the -Input pin on the package to maintain so small a parasitic capacitance, and a socket is probably too capacitive to use.

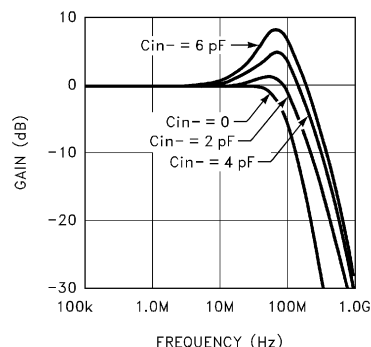


FIGURE 9. REALISTIC CMF RESPONSE WITH VARIOUS VALUES OF C_{IN-}

Settling Behavior

The small tolerated values of C_{IN-} scale with the effective C_{COMP} of the CMF amplifier. Higher values of feedback resistor require smaller C_{COMP} for a given natural bandwidth and thus less C_{IN-} can be tolerated. Since 1.5pF is a minimum practical value for the parasitic C_{IN-} , almost no CMF designs use R_F values greater than 1.3kΩ. Higher frequency amplifiers use R_F values around 300Ω to mitigate the C_{IN-} problem.

As shown in Figure 9, our natural bandwidth of 50MHz was expanded to a -3dB frequency of over 100MHz. This design is typical for the moderate supply current devices; there is not enough quiescent current to maximize the current mirror and output stage bandwidths. Higher supply current amplifiers or amplifiers built from very high-frequency IC processes have more bandwidth in the mirrors and output stage and display less peaking for a given bandwidth and give more reproducible frequency responses. Our definition of “moderate” supply current will again be CMF amplifiers that draw about 8mA–10mA; optimized amplifiers draw around 16mA.

The ratio of -3dB frequency to natural bandwidth is an interesting number. In high frequency circuits it is always greater than unity. The closer to unity this “Bandwidth Expansion” ratio is, the better-behaved the amplifier. That is,

a ratio close to one makes the CMF more tolerant to C_{IN-} and varying values of R_F , and it also makes the -3dB bandwidth at higher gains maximized. If the bandwidth ratio is high, say around 2, then the natural bandwidth of the amplifier is substantially lower than the unity-gain -3dB frequency, and the peaking which caused a -3dB bandwidth increase at unity gain fades and allows the more modest natural bandwidth to dominate the higher gains. Figure 11 shows this effect. The higher gains do not show peaking and the ideal bandwidth loss-vs.-gain relationship holds.

The higher-gain bandwidths can be made closer to the unity-gain -3dB frequency by reducing R_F . The strategy is to make the quantity $R_F + A_0 * R-$ constant by reducing R_F as A_0 increases. In our example, the natural bandwidth was based on $R_F + A_0 * R- = 1050\Omega$. At a gain of +10, we could reduce R_F to 550Ω and obtain maximum -3dB bandwidth.

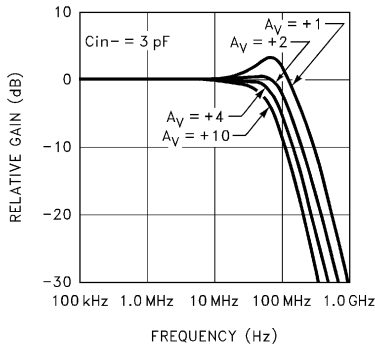


FIGURE 10. REALISTIC CMF RESPONSE WITH VARIOUS CLOSED-LOOP GAINS

The Inverting Connection

When the CMF amplifier is configured as an inverting operational amplifier, as shown in Figure 11, the ideal gain in this configuration is:

$$\frac{V_O}{V_{IN}} = -\frac{R_F}{R_G}$$

which we will term $-A_0$.

The precise expression for the fed-back gain is:

$$\frac{V_O}{V_N} = -A_0 * \frac{1}{1 + \frac{R_F + A_0 * R-}{R_{OL}}}$$

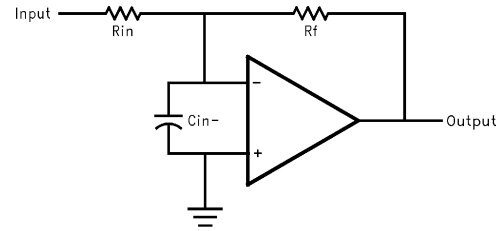


FIGURE 11. THE CMF CONNECTED AS AN INVERTING AMPLIFIER

The ideal gain error is close to that of the non-inverting case, and the ideal bandwidth also almost the same, with the A_0 term replaced by $(A_0 + 1)$. Because the amplifier inputs remain near ground as signals are passed, CMRR and -ICMR errors do not occur, and the ideal gain terms are maintained.

The inverting connection's input impedance is essentially R_{IN} . With $R_F = 1k\Omega$, a practical maximum gain for the inverting connection is about -20, since the input impedance drops to 50Ω . Even if the signal source could comfortably drive very low input impedances, simple interconnect inductances reduce bandwidths beyond 100MHz. The practical maximum gain is even less for CMF amplifiers that use lower value feedback resistors.

Another virtue of the inverting connection is that the sensitivity to C_{IN-} is substantially reduced. The inverting input is a virtual ground for low frequencies, and is a naturally low impedance $R-$ at medium and high frequencies. Thus, the signal magnitudes are low at the inverting input and little current will flow into a C_{IN-} to upset the ideal frequency response. Figure 12 shows our previous realistic CMF amplifier model's frequency responses with various values of C_{IN-} . Note the reduced peaking from C_{IN-} . With the flatter frequency response, the 0.1dB bandwidth improves, since the gain does not peak up and out of the ± 0.1 dB bound, as does the response of the non-inverting connection due to C_{IN-} . The -3dB bandwidth is usually less than that of the non-inverting connection because of the diminished peaking.

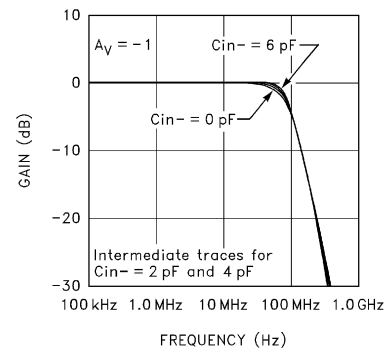


FIGURE 12. INVERTING CMF RESPONSE WITH VARIOUS VALUES OF C_{IN-}

It must be remembered that the input and output impedances of the integrated amplifiers are quite complex over frequency. The terminals themselves can exhibit resonances with connected impedances independent of feedback. These resonances will be exhibited generally between one and five times the natural bandwidth of the CMF amplifier. For instance, few amplifiers tolerate load capacitance well. Those that can tolerate capacitive loading are designed to simply “wimp out” at high frequencies and lose gain accuracy and load-driving capacity. Many amplifiers do not like to see inductive or high input impedances, and some amplifiers built with very high-frequency processes resonate with C_{IN} - even in the inverting mode. This term “resonance” can mean oscillation.

Noise

Noise performance of the CMF amplifier is characterized by four quantities, as shown in Figure 13. There is the typical input voltage noise V_n , generally placed in series with the +in terminal, the noises generated by R_F and R_G , and a noise current i_n which is peculiar to CMF amplifiers. This noise current is represented as being sent to the -in terminal from internal sources.

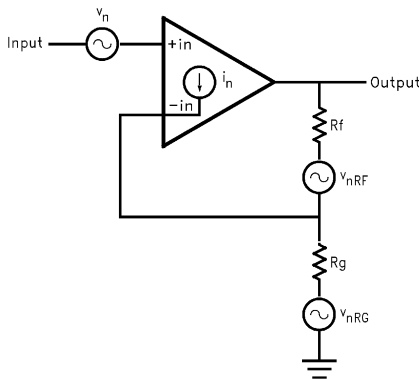


FIGURE 13. NOISE SOURCES IN A POSITIVE-GAIN CMF AMPLIFIER

For positive-gain connections, the noise contributions are so:

$$v_{in,total}^2 = v_n^2 + \left(\frac{4KTR_F}{A_V^2}\right) + \left(\frac{4KTR_G(A_V - 1)^2}{A_V^2}\right) + \left(\frac{i_n R_F}{A_V}\right)^2$$

Input-referred noise is in volts-squared per hertz here. K is the Boltzmann constant, and T is absolute temperature. The noise terms are, left to right, the -Input noise current, R_F resistor noise, R_G resistor noise, and input noise current. Note that all noise contributors except the input voltage noise itself reduce in magnitude as the gain A_V increases. Since R_G can be expressed in terms of R_F and A_V , we can simplify the expression:

$$v_{in,total}^2 = v_n^2 +$$

$$\left(\frac{4KTR_F}{A_V}\right) + \left(\frac{i_n R_F}{A_V}\right)^2$$

CMF amplifiers have low values of v_n , ranging from $2nV/\sqrt{Hz}$ to $8nV/\sqrt{Hz}$. A $1k\Omega$ resistor has a thermal noise of $4nV/\sqrt{Hz}$, a value that can be neglected at even modest gains. The current noise has values ranging from $10pA/\sqrt{Hz}$ to $40pA/\sqrt{Hz}$. A CMF amplifier designed to use a $1k\Omega$ feedback resistor would convert a typical $20pA/\sqrt{Hz}$ noise current to a $20nV/\sqrt{Hz}$ voltage, the largest term in the expression until A_V is greater than about 3.

Figure 14 shows the input-referred noise versus A_V for two CMF designs. One amplifier uses a $1k\Omega$ feedback resistor, and has a $6nV/\sqrt{Hz}$ input noise. The other is designed for a 250Ω feedback resistor and has a $4nV/\sqrt{Hz}$ input noise. Both amplifiers have a $20pA/\sqrt{Hz}$ noise current. The first amplifier is typical of lower-power designs; the second typical of the fastest designs. Clearly, the higher supply-current amplifiers that use low-value feedback resistors are the quietest.

At low frequencies, in the audio region, v_n and i_n have $1/F$ excess noise. For v_n , the $1/F$ corner is typically around $200Hz$. For i_n , it is typically at $2000Hz$. These $1/F$ extra noise quantities do not typically increase the total integrated noise voltage much, due to the large bandwidth beyond the audio frequencies that the CMF amplifier has to accumulate thermal noise over, but they do prevent instrumentation-quality DC performance.

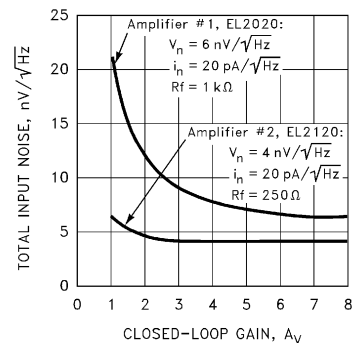


FIGURE 14. NOISE vs GAIN FOR TWO CMF AMPLIFIERS

Summary

The CMF amplifier has virtues unavailable in the traditional voltage-feedback design and it also has its own weaknesses. Enough variety exists among CMF products so that attention to individual amplifier characteristics is required to assure optimum circuit performance.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338