Designing High Current and High Power Density POL Converter Applications with Digital Power Modules

Introduction

Today’s latest FPGAs, processors, ASICs and associated memories in various industrial equipment have raised the performance requirement significantly on the point-of-load (POL) power converter solutions. To meet the increasing power demands and the shrinking real estate on the motherboard, advances have been made in POL power design to achieve both high current and high power density.

To ease the system design challenges associated with these advanced systems, high current and high power density modules are being developed. These modules include the controller, FETs, inductors, and the majority of the passives encapsulated in a single package, leaving only the input and output bulk capacitors outside to complete the system design. Enabled with advanced 3D integration and packaging technologies, integrated power module solutions can achieve much more superior performance over the conventional discrete solutions in terms of efficiency, thermal management and power density. This gives system engineers the advantage of more margin to power design specifications and faster time to market for new product development.

Thermal Management through Packaging

Thermal management is one of the greatest challenges in high power (greater than 100W) module design. Footprint and ultimate power rating, especially at high ambient temperature, are dictated by the module’s electrical and mechanical design. Using thermally enhanced packages that can efficiently move heat out of the package enables modules to deliver better thermal performance. In a highly integrated device such as a power module, the electrical and mechanical design is highly interdependent.

A power module is typically built upon a package substrate on which the semiconductor die and other electronic components are mounted and inter-connected. It is therefore imperative for this package substrate to provide good thermal conductivity. A variety of different types of package substrates are utilized in power modules. A dual layered printed circuit board (PCB) in a land grid array (LGA) power module provides a substrate with good routing capability and straightforward electrical interconnections. The thermal conductivity, however, is undesirably low and will penalize the module’s thermal performance. An alternative approach, using a metal lead frame on a quad flat no leads (QFN) package, provides very good thermal conductivity, but lacks the ease of routing capability. While the QFN can be modified to improve the routing, this technique usually results in higher package costs.

The best combination of thermal conductivity and routing capability is a single-layer conductive package substrate in a High Density lead-frame Array (HDA). This substrate comprises a peripheral and an interior portion. The peripheral portion includes contact pads used for surface mount on a motherboard while the interior portion includes floating contact pads that are electrically isolated from the peripheral contact pads and are coupled to internal components. The peripheral and interior contact pads of the HDA lead-frame, in combination with bond or jumper wires, allow the HDA power module to provide excellent routing capabilities, similar to that of a dual-layered PCB, as well as excellent thermal conductivity to dissipate heat because of the single conductive layer of material.
**3D Inductor Integration**

Inductor design is another critical piece of the electrical-mechanical design. Generally speaking, inductors must be designed sufficiently large to achieve low DC resistance (DCR) copper loss and core loss, while maintaining a reasonable operating temperature. Unfortunately, many applications have limited space on the motherboard such that an undersized inductor is often used. As a result, the designer either has to use a bulky heat sink or live with hot spot and poor efficiency.

A 3D stackable inductor structure addresses both the space and efficiency constraints. In this structure, the inductor can be designed almost as large as the entire power module footprint and installed over the other components. This technique significantly reduces the substrate area compared to a side-by-side mounting method, at the expense of a growth in package height. Thanks to the adequate budget of the inductor size, much smaller DCR loss and core loss can be easily achieved.

Figure 1 illustrates the cross-sectional view of two types of power module structures in concept. In Figure 1(A), a multi-layer PCB is utilized as the package substrate to provide flexibility of electrical interconnections and routings; the inductor is mounted side-by-side from the other components (controller, FETs, and passives). In this structure, and as noted earlier, the heat transfer efficiency can be poor due to the low thermal conductivity of the multi-layer substrate. With limited footprint space, it is often forced to use an undersized inductor. Since the inductor height dominates the module dimension in the Z-axis, any saving from the inductor’s X-Y dimensions could result in an increase of the inductor height and thus a waste of the module’s form factor.

In addition, the concentrated inductor structure also prevents efficient top and bottom side cooling. The advantageous HDA power module structure with 3D inductor integration is illustrated in Figure 1(B). The single-layer copper lead-frame with both the peripheral and interior portions (not shown) offers similar routing capabilities to a dual-layer PCB and a much higher thermal conductivity. By installing the inductor on top of other components, the space along the Z-axis is efficiently utilized. The module footprint area is reduced, while simultaneously minimizing the inductor DCR and core loss. Furthermore, heat concentration at the inductor is easily avoided due to the reduced inductor loss and effective large heat dissipation area.

![A. Power module structure with multi-layer substrate and side-by-side inductor mount](image)

![B. HDA power module using single-layer substrate and 3D inductor integration](image)

*Figure 1. Cross-sectional view of two types of power module structures*
**Design Example: 50A Digital PMBus Power Module**

Intersil’s ISL8272M is a 50A step-down PMBus-compliant digital power module, which offers the industry’s highest current capacity from a compact (18mm x 23mm x 7.5mm) HDA package. Dual phases are connected in parallel to deliver current through a single output. Figure 2 shows the typical 50A application diagram using ISL8272M.

The ISL8272M dual-phase inductor has a proprietary design utilizing the 3D integration technology. Two windings are built on a single core such that the magnetic flux of the two windings are partially cancelled, thus reducing both the inductor size and core loss. Phase-interleaving allows further reduction of input capacitors and output voltage ripples. Figure 3 shows the high efficiency performance of this structure.

![Typical 50A application diagram of the ISL8272M](image)

**Figure 2. Typical 50A application diagram of the ISL8272M**

![ISL8272M efficiency curves at $V_{IN}=12V$, $F_{SW}=300kHz$ for various output voltages](image)

**Figure 3. ISL8272M efficiency curves at $V_{IN}=12V$, $F_{SW}=300kHz$ for various output voltages**

In Figure 4, the ISL8272M’s power loss breakdown is compared with the traditional dual-phase 50A design incorporating two side-by-side mounted inductors. The total inductor loss of the ISL8272M can be reduced...
from 3W to 1.3W for a 12V input to 1V output at 50A load current application. Hence, the full load efficiency of ISL8272M reaches 88.3%, a much better figure than the 85.7% efficiency of traditional designs.

![Power Loss Comparison](image)

**Figure 4.** Power loss comparison between ISL8272M and the typical design with two separate inductors side-by-side. Operating conditions: $V_{IN}=12V$, $V_{OUT}=1V$, $I_{OUT}=50A$, $F_{SW}=533kHz$, $T_A=25^\circ C$.

Thermal images of the ISL8272M encapsulated digital power module running a continuous 50A load are shown in Figure 5. Mounted on a 2oz. 6-layer FR4 4.7 inch x 4.8 inch board, the ISL8272M performs outstandingly in a thermal test, providing a non-derated 50A capacity even under the worst case condition of a 14V input voltage to 5V output voltage conversion ratio. The module achieves an ultra-high power density of >1300W/in³.

![Thermal Images](image)

**Figure 5.** Thermal images of the ISL8272M. (A) $V_{IN}=12V$, $V_{OUT}=1V$, $I_{OUT}=50A$, $F_{SW}=300kHz$, $T_A=25^\circ C$, 0LFM (no air flow). (B) $V_{IN}=14V$, $V_{OUT}=5V$, $I_{OUT}=50A$, $F_{SW}=533kHz$, $T_A=25^\circ C$, 0LFM (no air flow).
Fast Digital Control Enabling Output Capacitor Reduction

Digital power management equips systems with real-time intelligence and flexibility. It allows automatic compensation for changes in load and temperature, dynamic voltage scaling, and frequency shifting. It also provides full telemetry and monitoring of the system operating parameters.

Most importantly, the PWM, loop control and feedback can be implemented digitally. Analog signals are converted to digital through analog-to-digital converters (ADCs) such that the PWM and feedback loops can be handled by digital-signal processors or computational state machines. This important differentiation from pure analog control offers the advantages of maintaining stability without the compromises on responsiveness from which analog control often suffers. Therefore, the output capacitance required for handling transient load events can be reduced with a fast digital control loop, further strengthening the power density from a system design viewpoint.

Although digital control offers advantages in the fast loop design, many manufacturers are not taking full advantage of what the technology offers and have, in many cases, simply implemented the core analog PWM techniques in digital form. Digital control makes it possible to build far more flexible control loops by incorporating n x F_{SW} (switching frequency) oversampling, multi-rate sampling, various types of digital filters for notching and phase shaping, and Fourier transform. Such features associated with complex digital signal processing are often not feasible with traditional analog control techniques.

In Figure 6, the control block diagrams of a typical Type III analog compensation and a fast response digital compensation are illustrated for comparison.
B. Digital compensation using fast sampling and FIR ripple filter with dual-edge modulator

**Figure 6. Analog vs. digital compensations for voltage mode controlled buck converter**

Type III analog compensation in voltage-mode controlled buck converters is widely adopted in the industry. Typically, the core of a Type III compensator is a transfer function with two zeros and three poles. As we know, the first pole near origin forms a high gain at low frequency for steady state regulation, while the second pole is to compensate the output capacitor ESR zero, and the third pole is to provide more attenuation for the high-frequency noises caused by switching ripples. Meanwhile, the two zeroes are used to shape the loop gain at cross over and boost phase to make the loop stable. Figure 6(A) shows the third pole separating from the rest of the Type III compensator.

The one-pole low pass filter removes the switching ripple noises from the PWM modulator to maintain stability. But on the other side, it inevitably introduces extra phase lag to the loop, limiting the loop bandwidth and response speed in order to have sufficient phase margin. The only way to achieve further improvement with this analog architecture is to employ variable-frequency switching techniques, using higher frequency when the voltage is changing rapidly. But this is undesirable for many systems that have stringent electromagnetic compatibility (EMC) demands. Fixed-frequency operation is required in such systems so that the noise spectrum can be tightly controlled.

An example of a fast response digital compensation architecture is shown in Figure 6(B). In this control loop, the ADC is over sampling at a frequency of \( n \times F_{SW} \), where \( n > 1 \). Therefore, the phase lag or group delay introduced by the analog-to-digital conversion is negligible for the loop stability. Because of the over sampling, it is feasible to design the core compensator \( G_c(z^{-1}) \) to have a similar frequency response to the two-zero two-pole compensator in Figure 6(A) in terms of loop gain and phase. But most importantly, the filter employed to attenuate the high frequency switching ripple noises can be designed uniquely by digital means and completely differentiated from the analog compensator’s single-pole low-pass filter in Figure 6(A).

Benefiting from the advantages of digital signal processing, a low-latency FIR ripple filter can be easily incorporated and all repetitive ripple elements are totally rejected. All that remains are the non-periodic elements in the waveform, including transient steps with little or no delay. This results more than 20dB of ripple reduction without a significant time delay, thus allowing higher gains and higher bandwidths. Figure 7 shows the superior performance of the fast FIR ripple filter compared with the analog single-pole, low-pass filter. Additionally, it is very easy to implement a dual-edge PWM in digital control, which offers faster transient response compared to the popularly used single-edge (trailing or leading) PWM in analog control.
Similarly, instead of using over sampling for the entire digital loop, it is also advantageous to use a multi-rate sampling technique if the loop consists of a slow path and a fast path. A uniform sampling rate can be used in the slow path to deal with the steady state regulation while over sampling is adopted in the fast path to handle high frequency transients. In this case, the aforementioned fast FIR ripple filter just needs to be placed in the fast path to allow higher gain and higher bandwidth.
Proprietary ChargeMode™ technology developed by Intersil uses a multi-rate sampling technique, which samples the error and computes the modulation signal multiple times during a switching period. This technology significantly reduces group delay and therefore supports very high bandwidth operation. The phase lag is significantly reduced due to the reduction of group delay. The ChargeMode technology also uses a dual-edge modulator, which outperforms other so-called ‘leading-edge’ or ‘trailing edge’ modulators in terms of total group delay.

The fast transient performance of the ChargeMode technology is demonstrated in Figure 8. Typically, it only takes one switching cycle to charge the inductor current to the steady state level upon load turn on, and 4~5 switching cycles to recover the output voltage during a load transient event.

Figure 8. Transient response of the ChargeMode™ control. $V_{\text{IN}}=6\text{V}$, $V_{\text{OUT}}=1.2\text{V}$, $I_{\text{OUT}}=0\text{A}-10\text{A}$, $F_{\text{SW}}=400\text{kHz}$, $L=400\text{nH}$, $C_{\text{OUT}}=570\mu\text{F}$
Enabled by the ChargeMode technology, the output capacitors required in the 50A digital power module system illustrated in Figure 2 can be much less than those required in the analog counterparts. High density is further guaranteed from the system level point of view.

**Conclusion**

To meet the requirements necessary in high current and high density POL designs, the latest digital power modules offer advantages in terms of thermal management, footprint and transient response through the latest advances in packaging, electromechanical design and digital power. Intersil’s ISL8272M 50A digital PMBus power module illustrates the advantages of these techniques. Innovations like ChargeMode technology are allowing system designers to rethink their POL design trade-offs so they can achieve both the higher power density, thermal performance and improved efficiency advanced systems require.

**Next Steps**

- [Learn more about the ISL8272M](#)
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