Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators

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Assumptions

This Technical Brief makes the following assumptions:

1. The power supply designer has already designed the power stage of the single phase buck converter. The last step to the design is the compensation network.
2. The designer has at least a basic understanding of control systems theory.
3. The designer has a basic understanding of Bode plots.

Introduction

Synchronous and non-synchronous buck regulators have three basic blocks that contribute to the closed loop system. These blocks consist of the modulator, the output filter, and the compensation network which closes the loop and stabilizes the system.

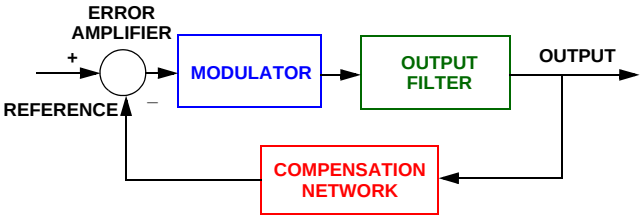


FIGURE 1. BASIC BLOCKS OF THE BUCK REGULATOR

Modulator

The modulator is shown in Figure 2. The input to the modulator is the output of the error amplifier, which is used to compare the output to the reference.

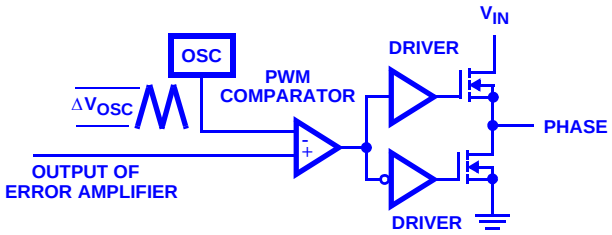


FIGURE 2. THE MODULATOR

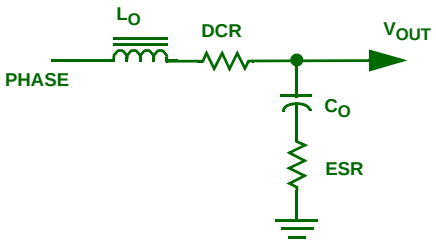
The output of the modulator is the PHASE node. The gain of the modulator is simply the input voltage to the regulator, V_{IN}, divided by the peak-to-peak voltage of the oscillator, ΔV_{OSC}, or:

$$GAIN_{MODULATOR} = \frac{V_{IN}}{\Delta V_{OSC}}$$

The peak to peak voltage of the oscillator can be obtained from the data sheet for the controller IC.

Output Filter

The output filter consists of the output inductor and all of the output capacitance. It is important to include the DC resistance (DCR) of the output inductor and the total Equivalent Series Resistance (ESR) of the output capacitor bank. The input to the output filter is the PHASE node and the output is the regulator output. Figure 3 shows the equivalent circuit of the output filter and its transfer function.



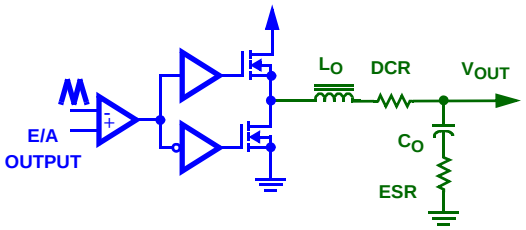
$$GAIN_{FILTER} = \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}}$$

FIGURE 3. THE OUTPUT FILTER

The transfer function for the output filter shows the well known double pole of an LC filter. It is important to note that the ESR of the capacitor bank and the DCR of the inductor both influence the damping of this resonant circuit. It is also important to notice the single zero that is a function of the output capacitance and its ESR.

Open Loop System

Figure 4 illustrates the open loop system and presents the transfer function.



$$GAIN_{OPENLOOP} = \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}}$$

FIGURE 4. THE OPEN LOOP SYSTEM

Figure 5 shows the asymptotic Bode plot of the open loop system gain.

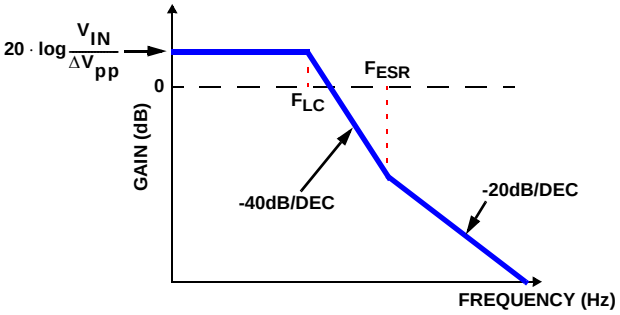


FIGURE 5. OPEN LOOP SYSTEM GAIN

Figure 5 represents a generic open loop system. Specific systems will have different double pole and ESR zero frequencies. For systems with very low DCR and ESR parameters, the phase will experience a very sharp slope downward at the double pole while the gain will have a rather high peak at the double pole. Systems that have such resonant output filters will be more difficult to compensate since the phase will need an extra boost to provide the necessary phase margin for stability. Systems such as this will typically need a Type III compensation, which will be discussed later in this brief.

Closing The Loop - The Compensation Network

Closing the control loop allows the regulator to adjust to load perturbations or changes in the input voltage which may adversely affect the output. Proper compensation of the system will allow for a predictable bandwidth with unconditional stability. In most cases, a Type II or Type III compensation network will properly compensate the system. The ideal Bode plot for the compensated system would be a gain that rolls off at a slope of -20dB/decade, crossing 0db at the desired bandwidth and a phase margin greater than 45^{o} for all frequencies below the 0dB crossing. For synchronous and non-synchronous buck converters, the bandwidth should be between 20 to 30% of the switching frequency.

Type II Compensation

Figure 6 shows a generic Type II compensation, its transfer function and asymptotic Bode plot. The Type II network helps to shape the profile of the gain with respect to frequency and also gives a 90^{o} boost to the phase. This boost is necessary to counteract the effects of the resonant output filter at the double pole.

If the output voltage of the regulator is not the reference voltage then a voltage programming resistor will be connected between the inverting input to the error amplifier and ground. This resistor is used to offset the output voltage to a level higher than the reference. This resistor, if present, has no effect on the compensation and can be ignored.

Figure 7 shows the closed loop system with a Type II compensation network and presents the closed loop transfer function.

The following guidelines will help calculate the poles and zeroes, and from those the component values, for a Type II network.

1. Choose a value for R_1, usually between 2k and 5kΩ.
2. Pick a gain (R_2/R_1) that will shift the Open Loop Gain up to give the desired bandwidth. This will allow the 0dB crossover to occur in the frequency range where the Type II network has a flat gain. The following equation will calculate an R_2 that will accomplish this given the system parameters and a chosen R_1.

$$R_2 = \left(\frac{F_{ESR}}{F_{LC}}\right)^2 \cdot \frac{DBW}{F_{ESR}} \cdot \frac{\Delta V_{OSC}}{V_{IN}} \cdot R_1$$

3. Calculate C_2 by placing the zero a decade below the output filter double pole frequency:

$$C_2 = \frac{10}{2\pi \cdot R_2 \cdot F_{LC}}$$

4. Calculate C_1 by placing the second pole at half the switching frequency:

$$C_1 = \frac{C_2}{\pi \cdot R_2 \cdot C_2 \cdot F_{sw} - 1}$$

Figure 8 shows the asymptotic Bode gain plot and the actual gain and phase equations for the Type II compensated system. It is recommended that the actual gain and phase plots be generated through the use of commercially available analytical software. Some examples of software that can be used are Mathcad, Maple, and Excel. The asymptotic plot of the gain and phase does not portray all the necessary information that is needed to determine stability and bandwidth.

The compensation gain must be compared to the open loop gain of the error amplifier. The compensation gain should not exceed the error amplifier open loop gain because this is the limiting factor of the compensation. Once the gain and phase plots are generated and analyzed, the system may need to be changed somewhat in order adjust the bandwidth or phase margin. Adjust the location of the pole and/or zero to modify the profile of the plots.

If the phase margin proves too difficult to correct, then a Type III system may be needed.

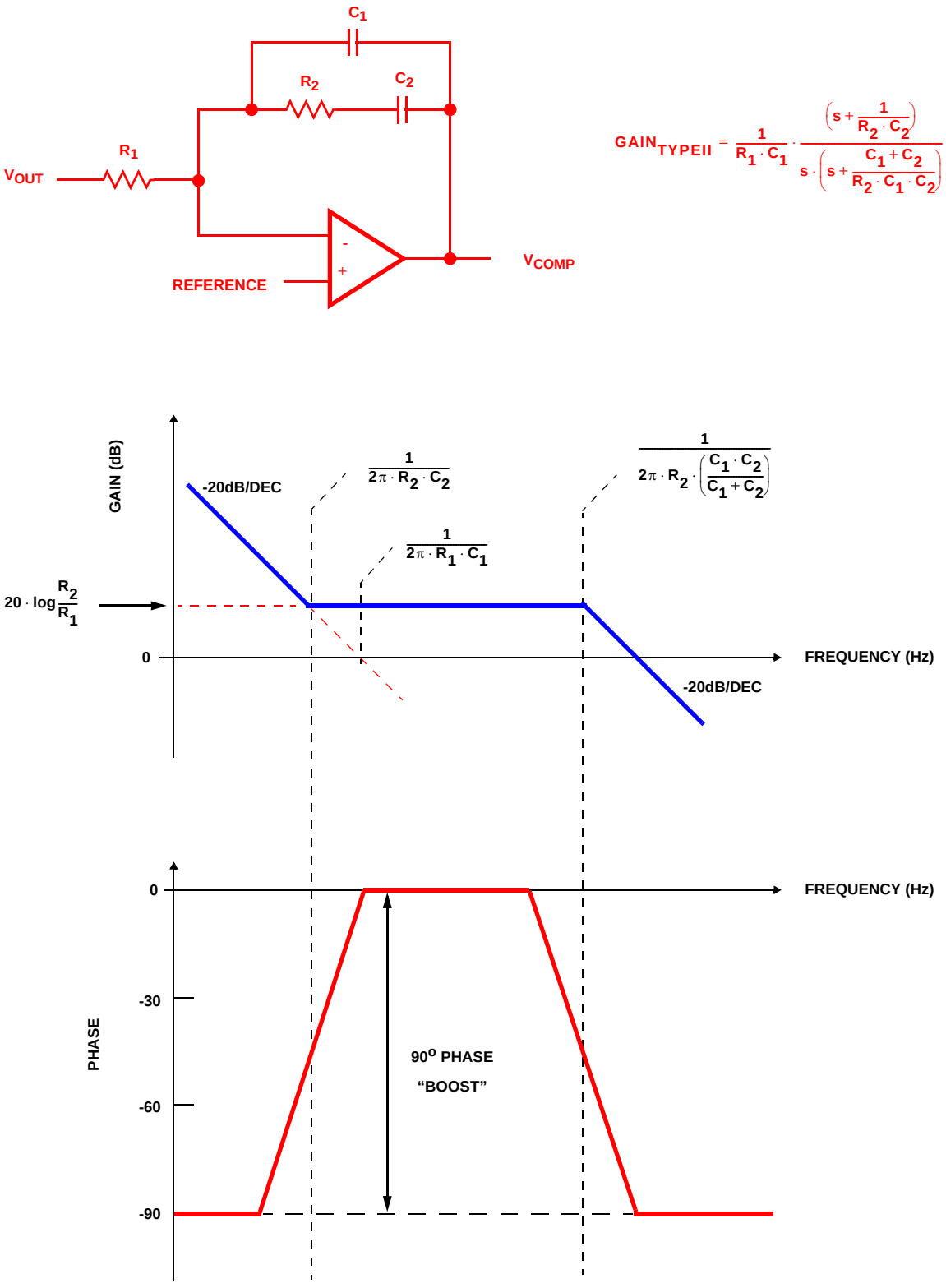
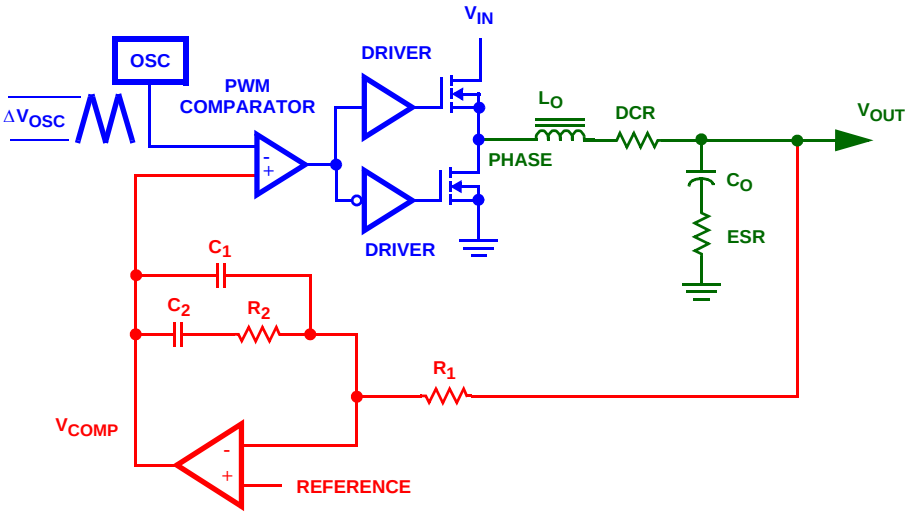
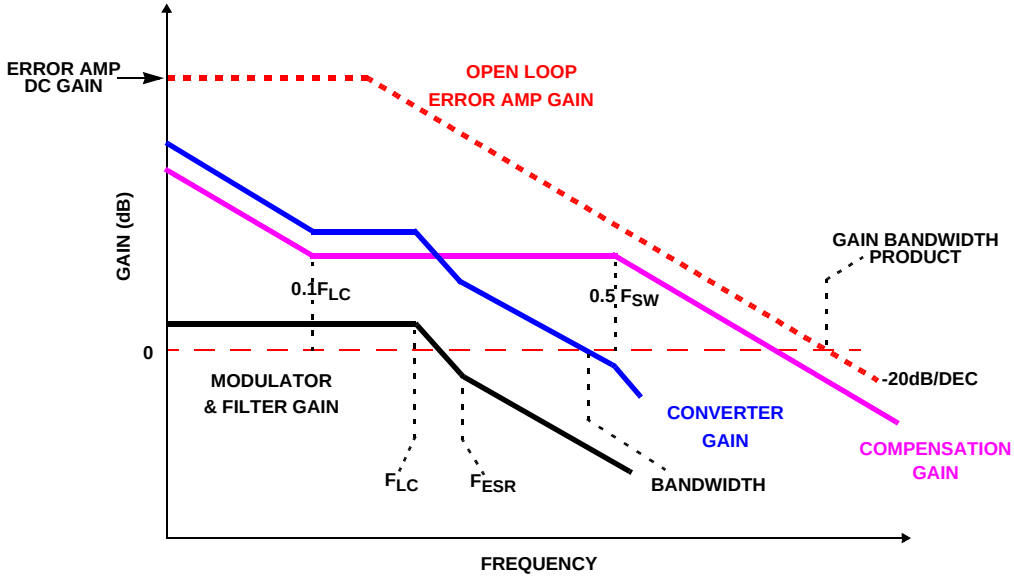


FIGURE 6. GENERIC TYPE II NETWORK



$$GAIN_{SYSTEM} = \frac{1}{R_1 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right)} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}}$$

FIGURE 7. CLOSED LOOP SYSTEM WITH TYPE II NETWORK



$$GAIN_{dB}(f) = GAIN_{MODULATOR} + GAIN_{FILTER} + GAIN_{TYPEII}$$

$$PHASE(f) = PHASE_{MODULATOR} + PHASE_{FILTER} + PHASE_{TYPEII}$$

Where:

$$GAIN_{MODULATOR} = 20 \cdot \log\left(\frac{V_{IN}}{\Delta V_{OSC}}\right)$$

$$GAIN_{FILTER} = 10 \cdot \log\left[1 + (2\pi f \cdot ESR \cdot C_{OUT})^2\right] - 10 \cdot \log\left[\left(1 - (2\pi f)^2 \cdot L_{OUT} \cdot C_{OUT}\right)^2 + (2\pi f \cdot (ESR + DCR) \cdot C_{OUT})^2\right]$$

$$PHASE_{FILTER} = \operatorname{atan}[2\pi f \cdot ESR \cdot C_{OUT}] + \operatorname{atan}\left[\frac{2\pi f \cdot ESR + DCR \cdot C_{OUT}}{2\pi f^2 \cdot L_{OUT} \cdot C_{OUT} - 1}\right]$$

$$GAIN_{TYPEII} = 10 \cdot \log\left[1 + (2\pi f \cdot R_2 \cdot C_2)^2\right] - 20 \cdot \log[2\pi f \cdot R_1 \cdot (C_1 + C_2)] - 10 \cdot \log\left[1 + \left(2\pi f \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)^2\right]$$

$$PHASE_{TYPEII} = -90^{o} + \operatorname{atan}[2\pi f \cdot R_2 \cdot C_2] - \operatorname{atan}\left[2\pi f \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right]$$

FIGURE 8. TYPE II COMPENSATED NETWORK

Type III Compensation

Figure 9 shows a generic Type III compensation, its transfer function and asymptotic Bode plot. The Type III network shapes the profile of the gain with respect to frequency in a similar fashion to the Type II network. The Type III network, however, utilizes two zeroes to give a phase boost of 180^{o}. This boost is necessary to counteract the effects of an under damped resonance of the output filter at the double pole.

Figure 10 shows the closed loop system with a Type III compensation network and presents the closed loop transfer function.

The guidelines for positioning the poles and zeroes and for calculating the component values are similar to the guidelines for the Type II network.

1. Choose a value for R_1, usually between 2k and 5kΩ.
2. Pick a gain (R_2/R_1) that will shift the Open Loop Gain up to give the desired bandwidth. This will allow the 0dB crossover to occur in the frequency range where the Type III network has its second flat gain. The following equation will calculate an R_2 that will accomplish this given the system parameters and a chosen R_1.

$$R_2 = \frac{DBW}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN}} \cdot R_1$$

3. Calculate C_2 by placing the zero at 50% of the output filter double pole frequency:

$$C_2 = \frac{1}{\pi \cdot R_2 \cdot F_{LC}}$$

4. Calculate C_1 by placing the first pole at the ESR zero frequency:

$$C_1 = \frac{C_2}{2 \cdot \pi \cdot R_2 \cdot C_2 \cdot F_{ESR} - 1}$$

5. Set the second pole at half the switching frequency and also set the second zero at the output filter double pole. This combination will yield the following component calculations:

$$R_3 = \frac{R_1}{\frac{F_{SW}}{2 \cdot F_{LC}} - 1}$$

$$C_3 = \frac{1}{\pi \cdot R_3 \cdot F_{SW}}$$

Figure 11 shows the asymptotic Bode gain plot for the Type III compensated system and the gain and phase equations for the compensated system. As with the Type II compensation network, it is recommended that the actual gain and phase plots be generated through the use of a commercially available analytical software package that has the capability to plot.

The compensation gain must be compared to the open loop gain of the error amplifier. The compensation gain should not exceed the error amplifier open loop gain because this is the limiting factor of the compensation. Once the gain and phase plots are generated the system may need to be changed after it is analyzed. Adjust the poles and/or zeroes in order to shape the gain profile and insure that the phase margin is greater than 45^{o}.

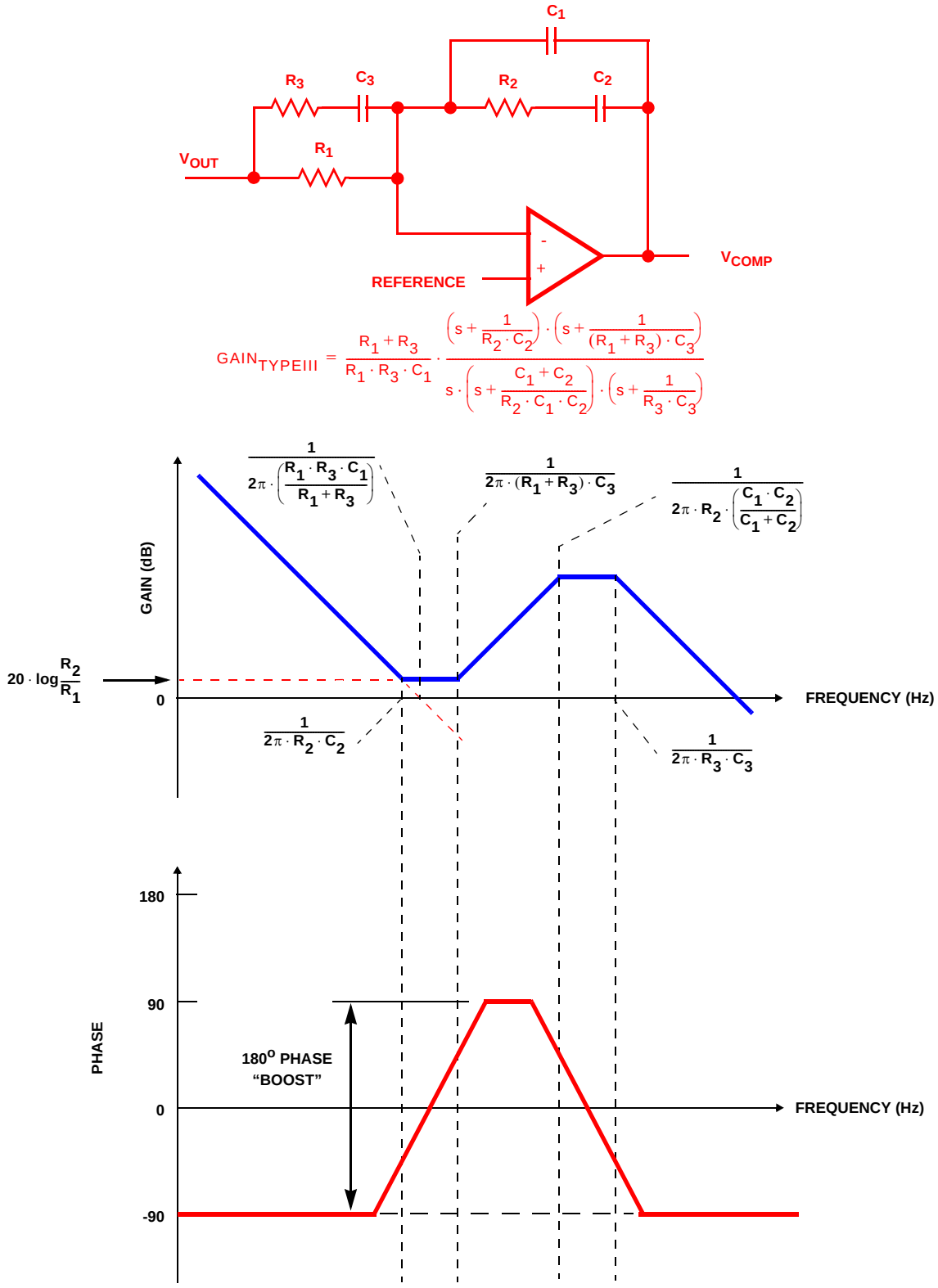
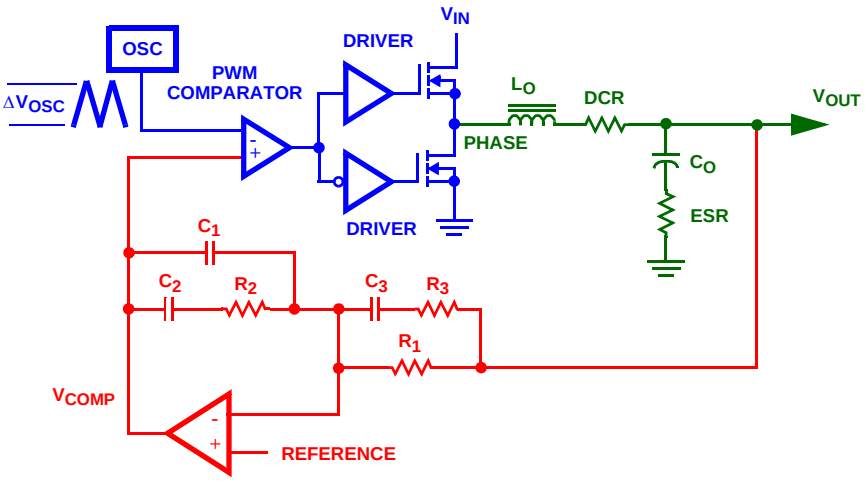


FIGURE 9. GENERIC TYPE III NETWORK



$$GAIN_{SYSTEM} = \frac{R_1 + R_3}{R_1 \cdot R_3 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right) \cdot \left(s + \frac{1}{(R_1 + R_3) \cdot C_3}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right) \cdot \left(s + \frac{1}{R_3 \cdot C_3}\right)} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}}$$

FIGURE 10. CLOSED LOOP SYSTEM WITH TYPE III NETWORK

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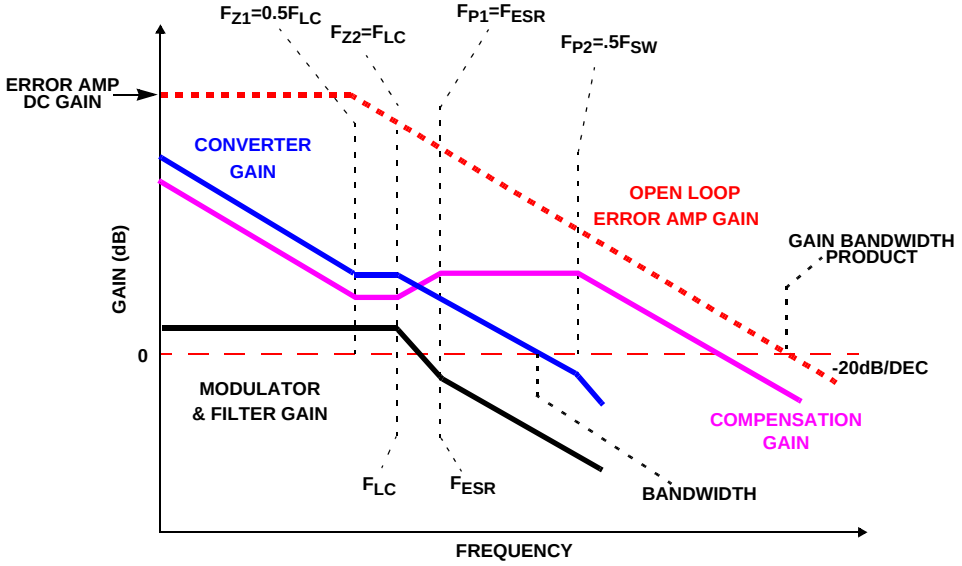


$$GAIN_{dB}(f) = GAIN_{MODULATOR} + GAIN_{FILTER} + GAIN_{TYPEIII}$$

$$PHASE(f) = PHASE_{MODULATOR} + PHASE_{FILTER} + PHASE_{TYPEIII}$$

Where: $$GAIN_{MODULATOR} = 20 \cdot \log\left(\frac{V_{IN}}{\Delta V_{OSC}}\right)$$

$$GAIN_{FILTER} = 10 \cdot \log\left[1 + (2\pi f \cdot ESR \cdot C_{OUT})^2\right] - 10 \cdot \log\left[\left(1 - (2\pi f)^2 \cdot L_{OUT} \cdot C_{OUT}\right)^2 + (2\pi f \cdot (ESR + DCR) \cdot C_{OUT})^2\right]$$

$$PHASE_{FILTER} = \operatorname{atan}[2\pi f \cdot ESR \cdot C_{OUT}] + \operatorname{atan}\left[\frac{2\pi f \cdot ESR + DCR \cdot C_{OUT}}{2\pi f^2 \cdot L_{OUT} \cdot C_{OUT} - 1}\right]$$

$$GAIN_{TYPEIII} = 10 \cdot \log\left[1 + (2\pi f \cdot R_2 \cdot C_2)^2\right] - 20 \cdot \log[2\pi f \cdot R_1 \cdot (C_1 + C_2)] - 10 \cdot \log\left[1 + \left(2\pi f \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)^2\right] + 10 \cdot \log\left[1 + (2\pi f \cdot (R_1 + R_3) \cdot C_3)^2\right] - 10 \cdot \log\left[1 + (2\pi f \cdot R_3 \cdot C_3)^2\right]$$

$$PHASE_{TYPEIII} = -90^o + \operatorname{atan}[2\pi f \cdot R_2 \cdot C_2] - \operatorname{atan}\left[2\pi f \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right] + \operatorname{atan}[2\pi f \cdot (R_1 + R_3) \cdot C_3] - \operatorname{atan}[2\pi f \cdot R_3 \cdot C_3]$$

FIGURE 11. TYPE III COMPENSATED NETWORK

Example

The following example will illustrate the entire process of compensation design for a synchronous buck converter.

Converter Parameters

Input Voltage:	V_{IN}	5V
Output Voltage:	V_{OUT}	3.3V
Controller IC:	IC	ISL6520A
Osc. Voltage:	ΔV_{OSC}	1.5V
Switching Frequency:	f_{SW}	300kHz
Total Output Capacitance:	C_{OUT}	990µF
Total ESR:	ESR	5mΩ
Output Inductance:	L_{OUT}	900nH
Inductor DCR:	DCR	3mΩ
Desired Bandwidth:	DBW	90kHz

First, a Type II compensation network will be attempted. The low ESR of the output capacitance and the low DCR of the output inductor may make the implementation of a Type II network difficult.

The guidelines given for designing a Type II network were followed in order to calculate the following component values:

R_1 = 4.12kΩ (chosen as the feedback component)
R_2 = 125.8kΩ
C_1 = 8.464pF
C_2 = 2.373nF

These calculated values need to be replaced by standard resistor values before the gain and phase plots can be plotted and examined.

R_1 = 4.12kΩ
R_2 = 124kΩ
C_1 = 8.2pF
C_2 = 2.2nF

Upon analysis of the bode plots in Figure 12, it can be seen that the system does not meet the stability criteria previously set. The bode plot for the gain is acceptable. The gain rolls off at 20dB/decade with a perturbation at the resonant point of the LC filter. After the perturbation, the gain again begins to roll off about 20dB/decade until it crosses 0dB right around 90kHz. The phase plot shows the problem with this Type II system. The low ESR and DCR values create a very sharp slope downward at the double pole of the LC filter.

The dive in the phase is so sharp that the 90^o phase boost of the Type II network does not compensate the phase enough to have sufficient phase margin. At approximately 6kHz, the phase margin goes below 45^o and never recovers. There is nothing more that the Type II system can do to improve the phase. The Phase of the compensation is at it's peak when the phase of the filter is at it's minimum.

Another problem with the Type II compensation network in this example is that the compensation gain intersects and then exceeds the gain of the error amplifier open loop gain. As the open loop gain of the error amplifier is the limiting factor to the compensation gain, the actual gain and phase is affected by the limit and will not exceed it.

Due to these issues, a Type III network will need to be implemented to compensate for the phase properly.

The guidelines for the Type III network were then followed to produce the following component values:

R_1 = 4.12kΩ (chosen as the feedback component)
R_2 = 20.863kΩ
R_3 = 151.85Ω
C_1 = 0.2587nF
C_2 = 2.861nF
C_3 = 6.987nF

Again, these calculated values need to be replaced by standard resistor values before the gain and phase plots can be plotted and examined.

R_1 = 4.12kΩ
R_2 = 20.5kΩ
R_3 = 150Ω
C_1 = 0.22nF
C_2 = 2.7nF
C_3 = 6.8nF

The gain plot of the Type III compensated system in Figure 13 looks very good. The gain rolls off at -20dB/decade from low frequency all the way to the 0dB crossover with a small perturbation from the LC filter double pole resonant point. The phase plot shows a system that is unconditionally stable.

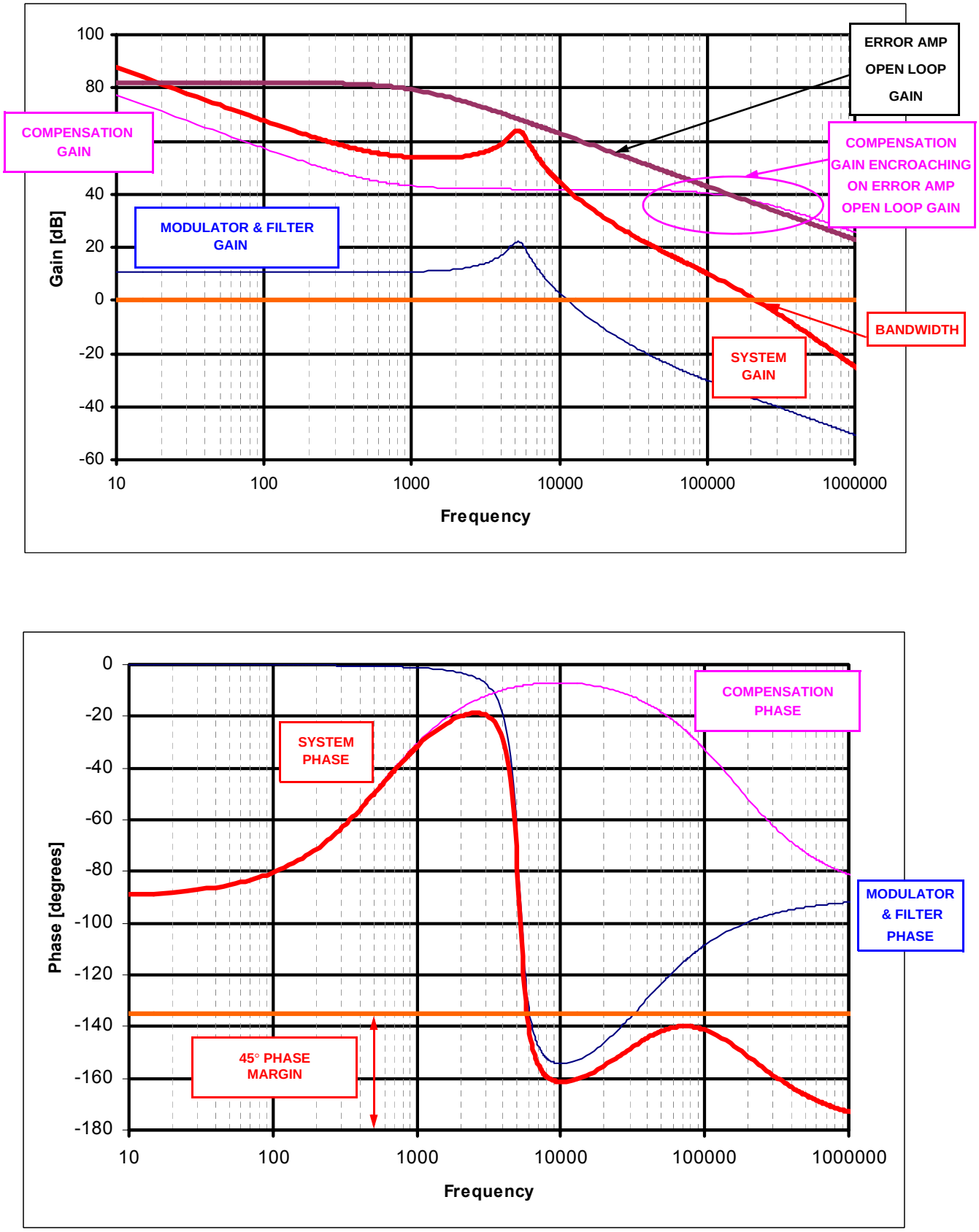
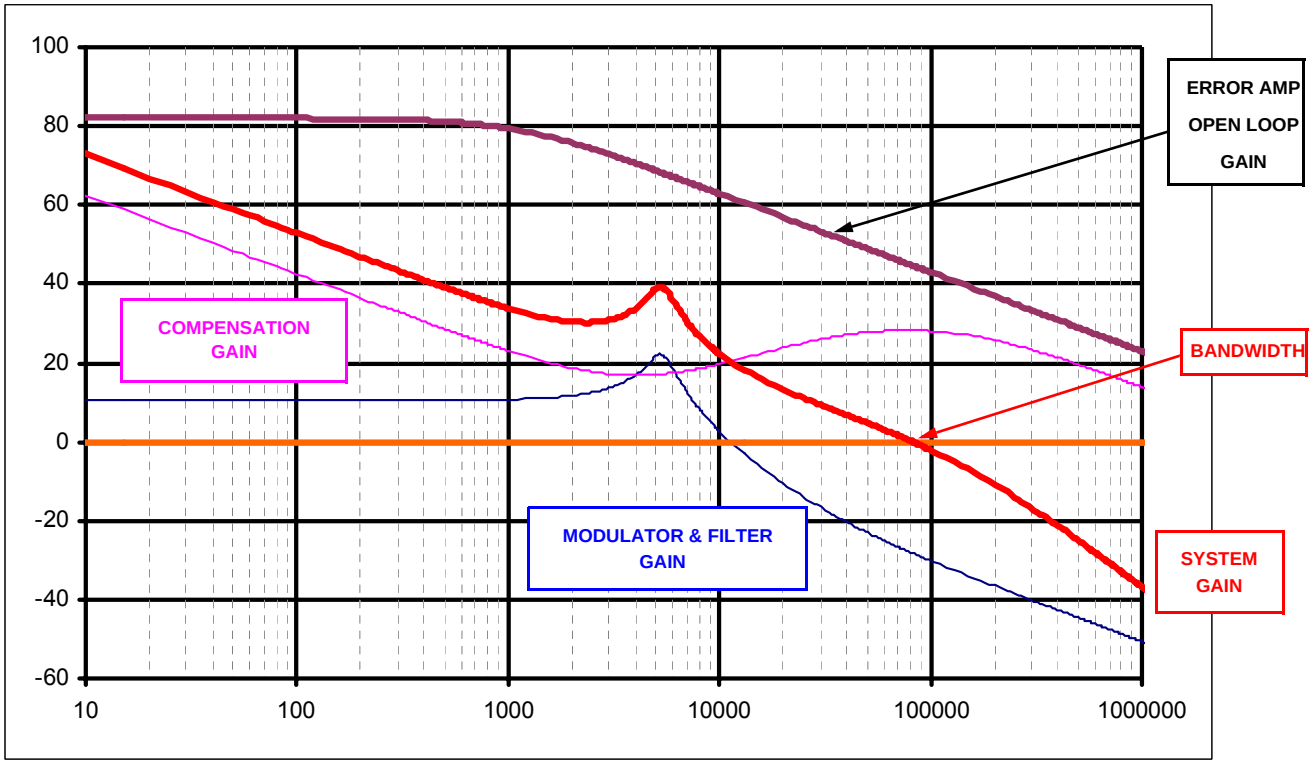


FIGURE 12. BODE PLOT OF THE TYPE II SYSTEM EXAMPLE



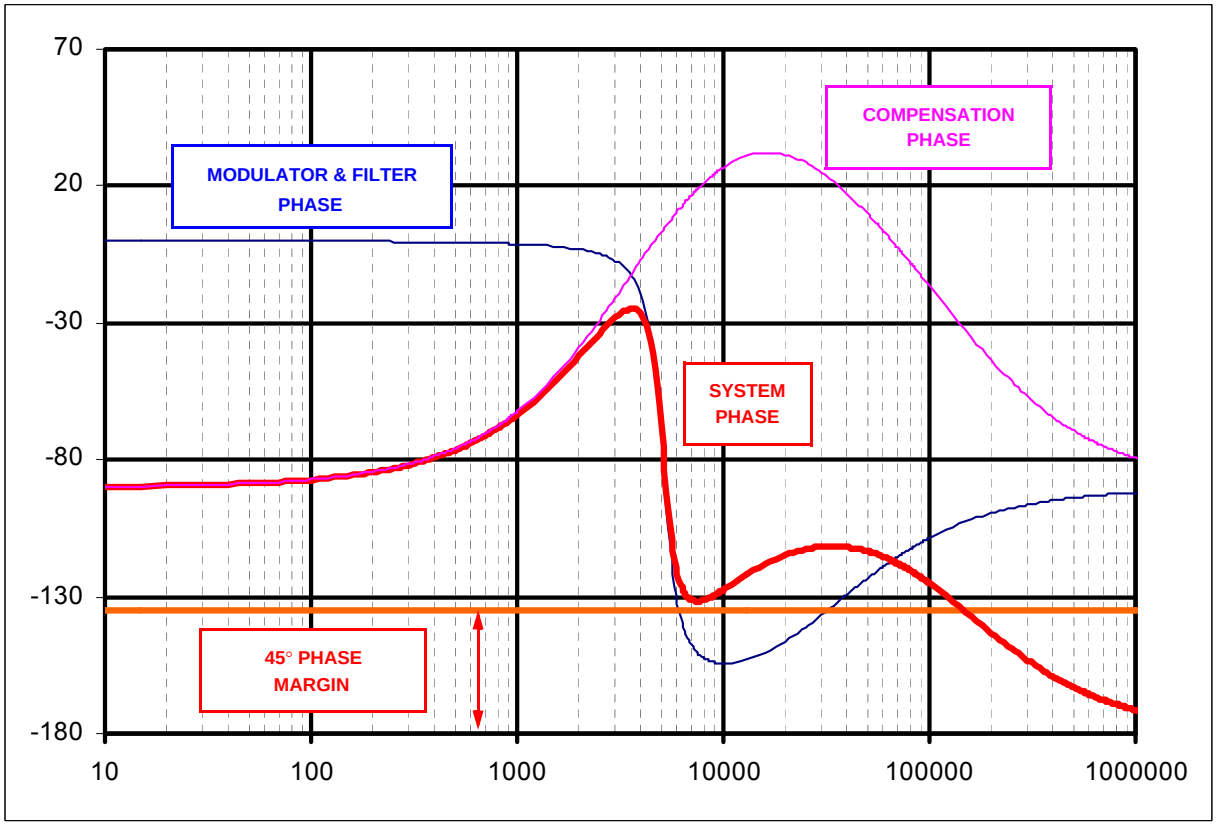


FIGURE 13. BODE PLOT OF THE TYPE III SYSTEM EXAMPLE