ISL9120IR

Compact High Efficiency Low Power Buck-Boost Regulator

FN8743
Rev 1.00
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The ISL9120IR is a highly integrated buck-boost switching regulator that accepts input voltages either above or below the regulated output voltage. This regulator automatically transitions between buck and boost modes without significant output disturbance. The ISL9120IR also has automatic bypass functionality for when the input voltage is generally within 1% to 2% of the output voltage, there will be a direct bypass connection between the VIN and VOUT pins. In addition to the automatic bypass functionality, the ISL9120IR also has a forced bypass functionality with the use of the BYPS pin.

This device is capable of delivering up to 800mA of output current (V_{IN} = 2.5V, V_{OUT} = 3.3V) and provides excellent efficiency due to its adaptive current limit pulse frequency modulation (PFM) control architecture.

The ISL9120IR is designed for stand-alone applications and supports a 3.3V fixed output voltage or variable output voltages with an external resistor divider. The forced bypass power saving mode can be chosen if voltage regulation is not required. The device consumes less than 3.5µA of current over the operating temperature range in the forced bypass mode.

The ISL9120IR requires only a single inductor and very few external components. Power supply solution size is minimized by a 3mmx3mm 12 Ld TQFN package.

Features

- Accepts input voltages above or below regulated output voltage
- Automatic bypass mode functionality
- Automatic and seamless transitions between buck and boost modes
- Input voltage range: 1.8V to 5.5V
- Selectable forced bypass power saving mode
- Adaptive multilevel current limit scheme to optimize efficiency at low and high currents
- Output current: up to 800mA (V_{IN} = 2.5V, V_{OUT} = 3.3V)
- High efficiency: up to 98%
- 41µA quiescent current maximizes light-load efficiency
- Fully protected for over-temperature and undervoltage
- Small 3mmx3mm 12 Ld TQFN package

Applications

- Smartphones and tablets
- Portable consumer and wearable devices

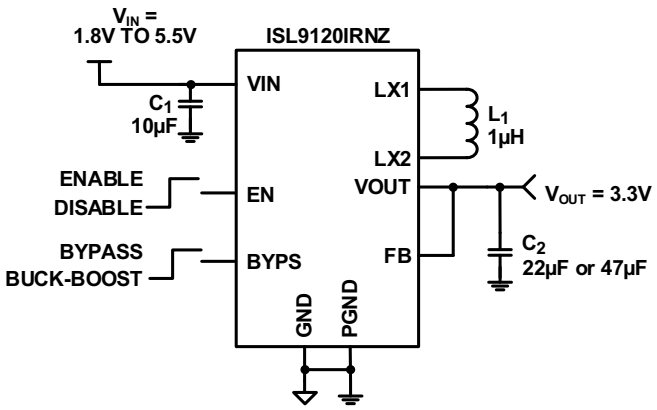


FIGURE 1. TYPICAL FIXED OUTPUT APPLICATION

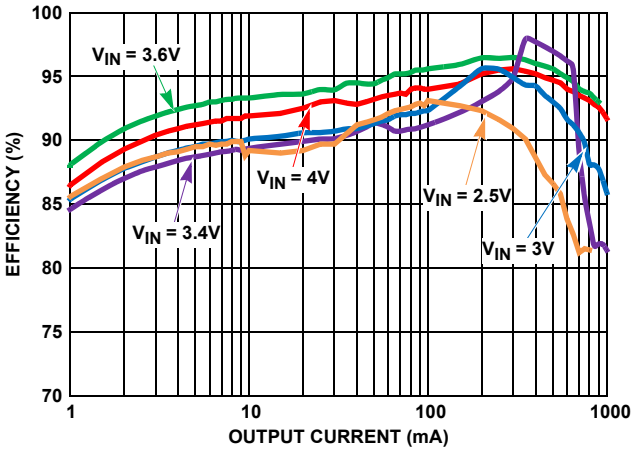


FIGURE 2. EFFICIENCY: V_{OUT} = 3.3V, T_A = +25°C

Block Diagram

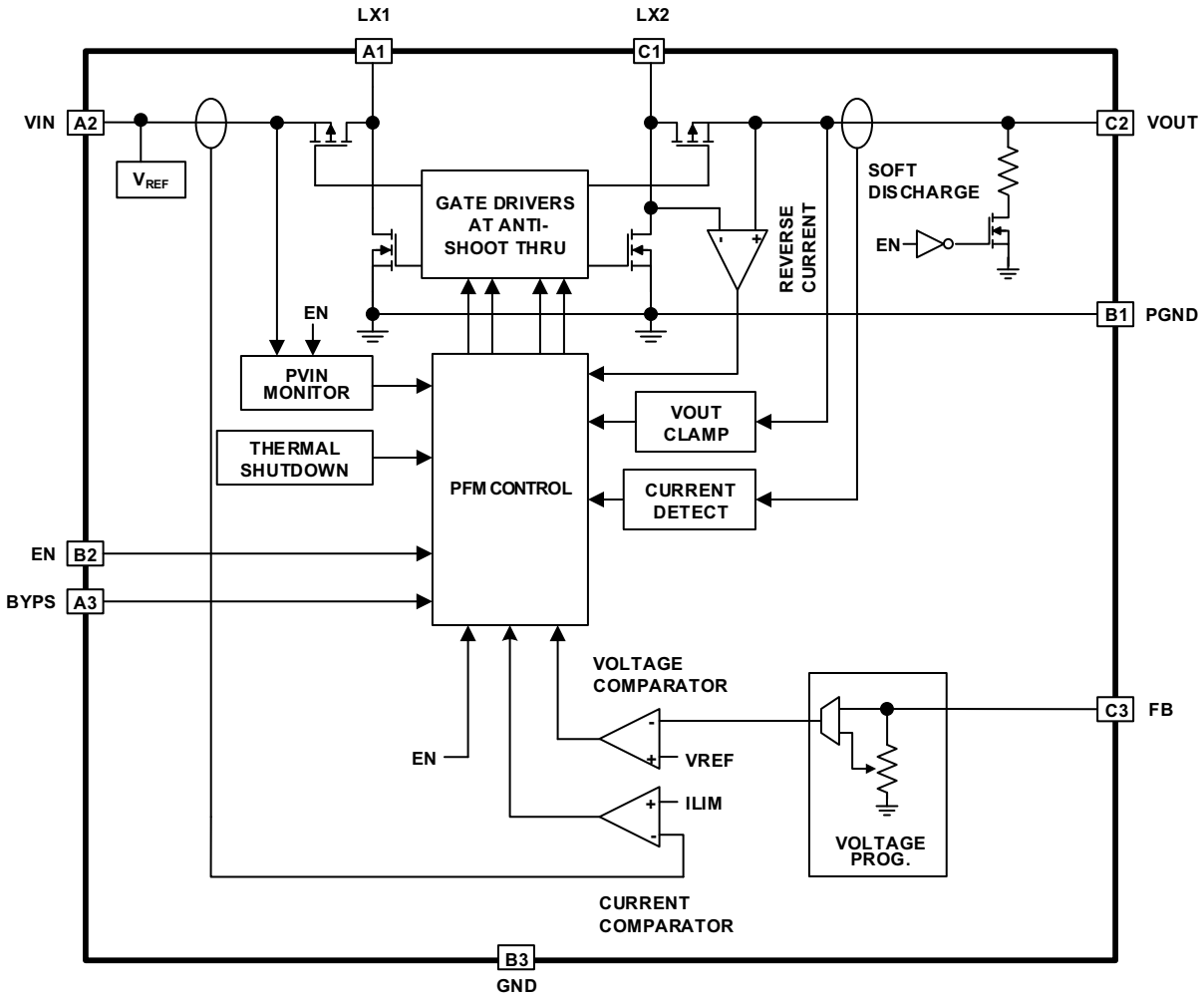
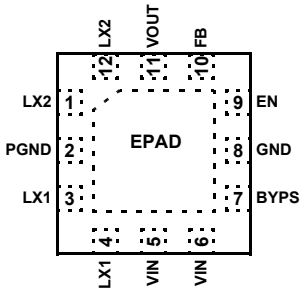


FIGURE 3. BLOCK DIAGRAM

Pin Configuration

ISL9120IR
(12 LD 3x3 TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 12	LX2	Inductor connection, output side.
2	PGND	Power ground for high switching current.
3, 4	LX1	Inductor connection, input side.
5, 6	VIN	Power supply input. Range: 1.8V to 5.5V. Connect 1x 10µF capacitor to PGND.
7	BYPS	Bypass mode enable pin. HIGH for bypass mode. LOW for buck-boost mode.
8	GND	Analog ground pin.
9	EN	Logic input, drive HIGH to enable device.
10	FB	Voltage feedback pin.
11	VOUT	Buck-boost output. Connect 22µF or 47µF capacitor to PGND.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	VOUT (V)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL9120IRTAZ	120A	ADJ.	-40 to +85	12 Ld 3x3 TQFN	L12.3x3A
ISL9120IRTNZ	120N	3.3	-40 to +85	12 Ld 3x3 TQFN	L12.3x3A
ISL9120IRN-EVZ	Evaluation Board for ISL9120IRNZ				
ISL9120IRA-EVZ	Evaluation Board for ISL9120IRAZ				

NOTES:

1. Add “-T*” suffix for 3k unit tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL9120. For more information on MSL, please see tech brief TB363.

FIGURE 4. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

	ISL9120	ISL9120IR
Buck-boost regulation	Yes	Yes
Bypass	Yes	Yes
Package	1.41x1.41mm 9-Bump WLCSP	3x3mm 12Ld TQFN

Absolute Maximum Ratings

VIN . . . . . -0.3V to 6.5V
LX1, LX2. . . . . -0.3V to 6.5V
FB . . . . . -0.3V to 6.5V
GND, PGND . . . . . -0.3V to 0.3V
All Other Pins . . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2.5kV
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (Tested per JESD22-C101F). 2kV
Latch-Up (Tested per JESD78D; Class 2) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
3x3 TQFN (Notes 4, 5)	55	5

Maximum Junction Temperature . . . . . +125°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Supply Voltage (V_{IN}) Range . . . . . 1.8V to 5.5V
Load Current (I_{OUT}) Range (DC) . . . . . 0A to 800mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Analog Specifications

$V_{IN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, $L_1 = 1\mu H$, $C_1 = 10\mu F$, $C_2 = 47\mu F$, $T_A = +25°C$. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V).**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
POWER SUPPLY						
V_{IN}	Input Voltage Range		**1.8**		**5.5**	V
V_{UVLO}	V_{IN} Undervoltage Lockout Threshold	Rising		1.725	**1.790**	V
		Falling	**1.550**	1.650		V
I_{VIN}	VIN Supply Current	V_{OUT} = 3.7V (Note 7)		41	**55**	µA
I_{SD}	VIN Supply Current, Shutdown	EN = GND		0.005	**1**	µA
I_{BYP}	VIN Supply Current, Bypass Mode	BYPS = Logic High, $V_{IN} \leq 5V$		0.8	**3.5**	µA
OUTPUT VOLTAGE REGULATION						
V_{OUT}	Output Voltage Range	ISL9120IRAZ, I_{OUT} = 100mA	**1.00**		**5.20**	V
	Output Voltage Accuracy	V_{IN} = 3.7V, I_{OUT} = 1mA	**-3**		**+4**	%
V_{FB}	FB Pin Voltage Regulation	For adjustable output version (ISL9120IRAZ)		0.80		V
I_{FB}	FB Pin Bias Current	For adjustable output version (ISL9120IRAZ)			**0.025**	µA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation, 500mA	I_{OUT} = 500mA, V_{OUT} = 3.3V, V_{IN} step from 2.3V to 5.5V		0.00681		mV/mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation, 500mA	V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} step from 0mA to 500mA		0.0072		mV/mA
$\Delta V_{OUT}/\Delta V_I$	Line Regulation, 100mA	I_{OUT} = 100mA, V_{OUT} = 3.3V, V_{IN} step from 2.3V to 5.5V		0.00273		mV/mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation, 100mA	V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} step from 0mA to 100mA		0.05		mV/mA
V_{CLAMP}	Output Voltage Clamp	Rising	**5.32**		**5.82**	V
	Output Voltage Clamp Hysteresis			400		mV
DC/DC SWITCHING SPECIFICATIONS						
$I_{PFETLEAK}$	LX1 Pin Leakage Current		**-0.05**		**+0.05**	µA
$I_{NFETLEAK}$	LX2 Pin Leakage Current	V_{IN} = 3.6V	**-0.05**		**+0.05**	µA

Analog Specifications $V_{IN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, $L_1 = 1\mu H$, $C_1 = 10\mu F$, $C_2 = 47\mu F$, $T_A = +25°C$. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V). (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SOFT-START AND SOFT DISCHARGE						
t_{SS}	Soft-Start Time	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in buck mode. $V_{IN} = 4V$, $I_{OUT} = 500mA$		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in boost mode. $V_{IN} = 3V$, $I_{OUT} = 500mA$		1		ms
r_{DISCHG}	V_{OUT} Soft-Discharge ON-Resistance	$EN < V_{IL}$		110		Ω
POWER MOSFET						
r_{DSON_P}	P-Channel MOSFET ON-Resistance	$I_{OUT} = 200mA$, measured with internal test mode		63		mΩ
r_{DSON_N}	N-Channel MOSFET ON-Resistance	$I_{OUT} = 200mA$, measured with internal test mode		63		mΩ
INDUCTOR PEAK CURRENT LIMIT						
I_{LIM_MAX}	Maximum Peak Current Limit			2		A
THERMAL PROTECTION						
	Thermal Shutdown			150		°C
	Thermal Shutdown Hysteresis			35		°C
LOGIC INPUTS						
I_{LEAK}	Input Leakage			0.013	**0.500**	µA
V_{IH}	Input HIGH Voltage		**1.4**			V
V_{IL}	Input LOW Voltage				**0.4**	V

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Quiescent current measurements are taken when the output is not switching.

Typical Performance Curves

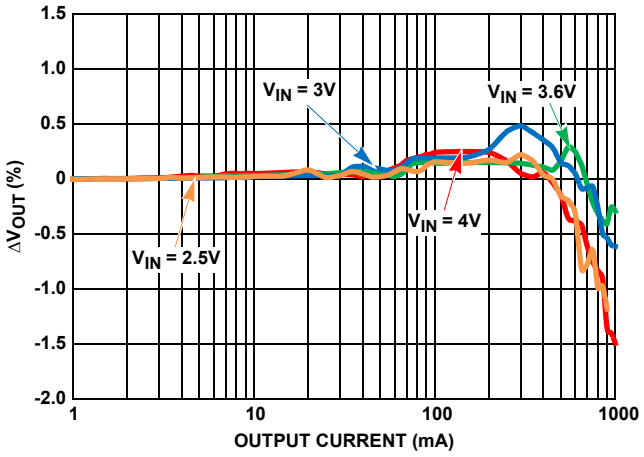


FIGURE 5. OUTPUT VOLTAGE vs LOAD CURRENT

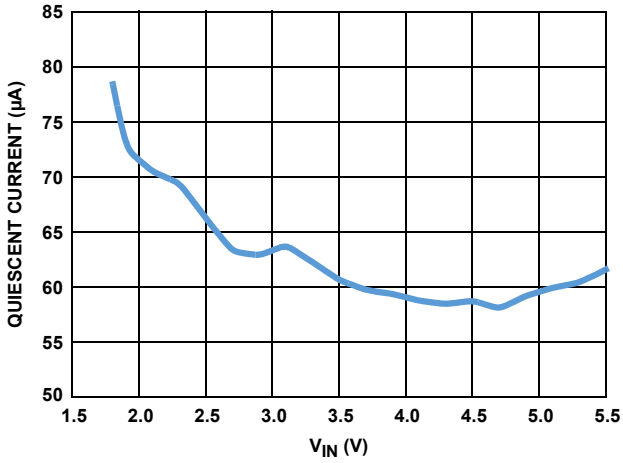


FIGURE 6. QUIESCENT CURRENT vs INPUT VOLTAGE (EN = HIGH)

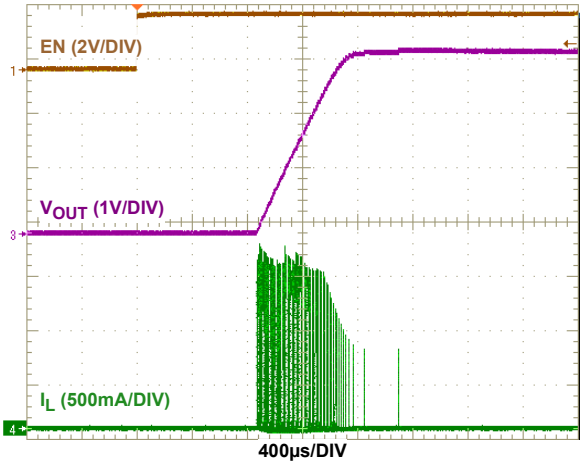


FIGURE 7. SOFT-START (V_{IN} = 4V, V_{OUT} = 3.3V, NO LOAD)

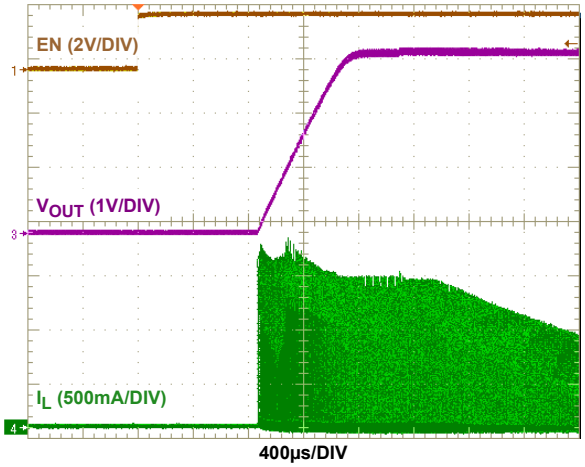


FIGURE 8. SOFT-START (V_{IN} = 4V, V_{OUT} = 3.3V, 0.5A R_{LOAD})

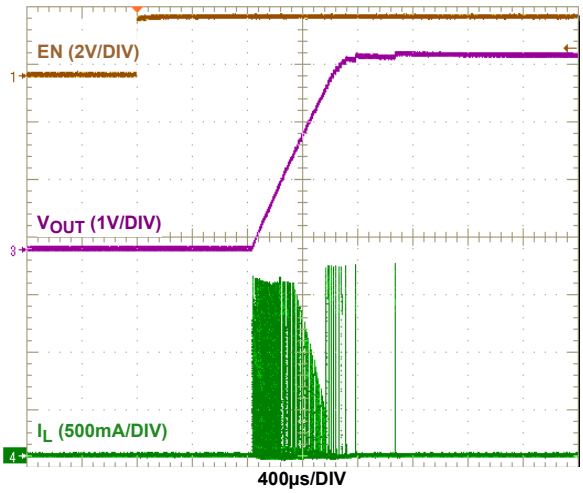


FIGURE 9. SOFT-START (V_{IN} = 3V, V_{OUT} = 3.3V, NO LOAD)

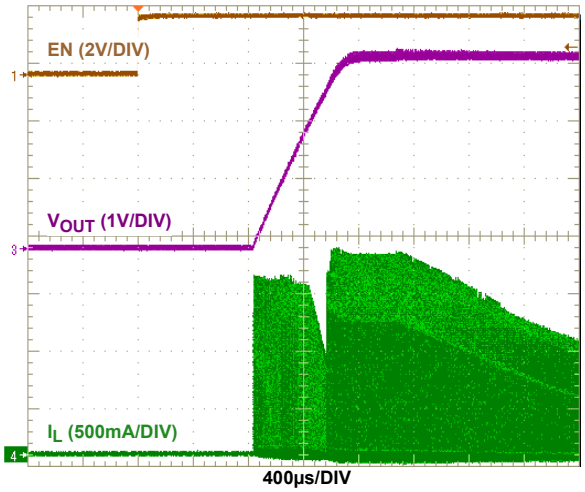


FIGURE 10. SOFT-START (V_{IN} = 3V, V_{OUT} = 3.3V, 0.5A R_{LOAD})

Typical Performance Curves (Continued)

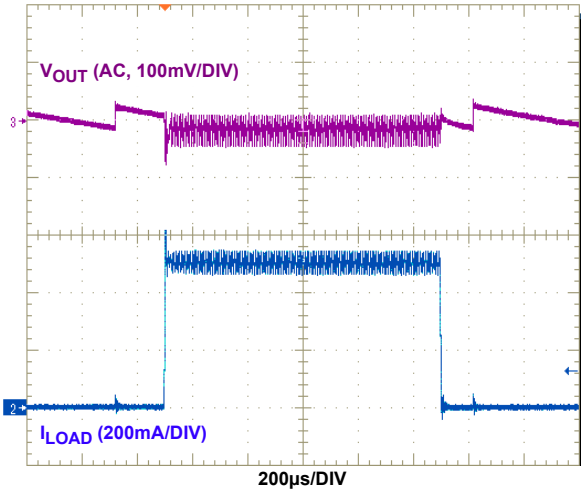


FIGURE 11. 0A TO 0.5A LOAD TRANSIENT (V_{IN} = 4V, V_{OUT} = 3.3V)

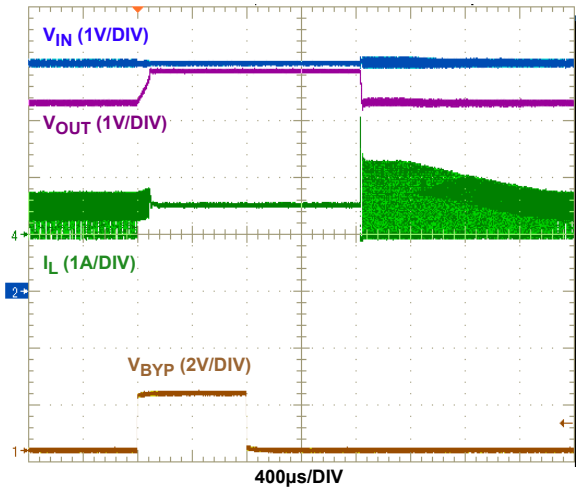


FIGURE 12. BYPASS FUNCTIONALITY (V_{IN} = 4V, V_{OUT} = 3.3, 0.5A R_{LOAD})

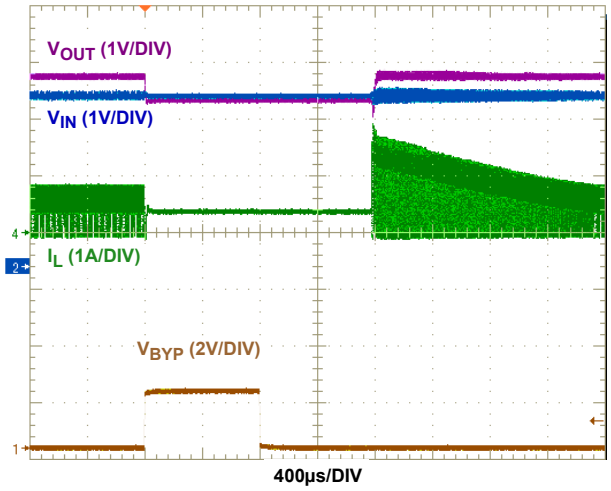


FIGURE 13. BYPASS FUNCTIONALITY (V_{IN} = 3V, V_{OUT} = 3.3, 0.5A R_{LOAD})

Functional Description

Functional Overview

Refer to the "Block Diagram" on page 2. The ISL9120IR implements a complete buck-boost switching regulator with a PFM controller, internal switches, references, protection circuitry and control inputs.

The PFM controller automatically switches between buck and boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads.

Internal Supply and References

Referring to the "Block Diagram" on page 2, the VIN pin supplies input power to the DC/DC converter and also provides the operating voltage source required for stable V_{REF} generation. Separate ground pins (GND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin, EN, allows the device to be enabled. Driving EN logic low invokes a power-down mode, where most internal device functions, including input and output power-good detection, are disabled.

Bypass Input

The BYPS pin allows the device to provide a direct connection from the VIN pin to the VOUT pin. The connection between the VIN and VOUT pins is through the external inductor and two internal power transistors. This function, called forced bypass mode operation, provides a very low quiescent current state.

For forced bypass mode operation, the minimum time required while in forced bypass operation is 800µs. Also when exiting forced bypass operation, the minimum time required before reentering forced bypass mode operation is 1ms.

Soft Discharge

When the device is disabled by driving EN logic low, an internal resistor between the VOUT and GND pins is activated. This internal resistor has a typical resistance of 110Ω.

POR Sequence and Soft-Start

Bringing the EN pin logic high allows the device to power-up. A number of events occur during the start-up sequence. The internal voltage reference powers up and stabilizes. The device then starts operating. There is a 1ms (typical) delay between assertion of the EN pin and the start of the switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping output voltage.

When the target output voltage is higher than the input voltage, there will be a transition from buck mode to boost mode during the soft-start sequence. At the time of this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

Undervoltage Lockout

The Undervoltage Lockout (UVLO) feature prevents abnormal operation in the event that the supply voltage is too low to guarantee proper operation. When the VIN pin voltage falls below the UVLO threshold, the regulator is disabled.

Thermal Shutdown

A built-in thermal protection feature protects the ISL9120IR if the die temperature reaches +150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal shutdown mode. When the die temperature falls to +115°C (typical), the device will resume normal operation.

When exiting thermal shutdown, the ISL9120IR will execute its soft-start sequence.

Buck-Boost Conversion Topology

The ISL9120IR operates in either buck or boost mode. When operating in conditions where V_{IN} is close to V_{OUT}, the ISL9120IR alternates between buck mode, boost mode and automatic bypass modes of operation as necessary to provide a regulated output voltage.

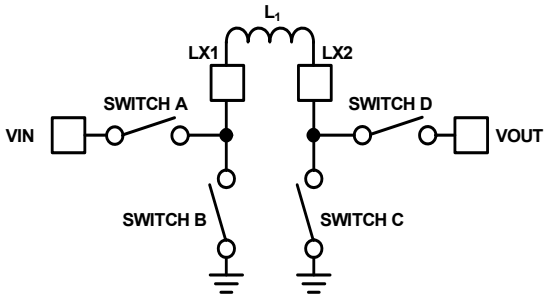


FIGURE 14. BUCK-BOOST TOPOLOGY

Figure 14 shows a simplified diagram of the internal switches and external inductor.

PFM Operation

During PFM operation in buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation. During PFM operation in boost mode, the ISL9120IR closes Switch A and Switch C to ramp-up the current in the inductor. When inductor current reaches the current limit, the device turns OFF Switches A and C, then turns ON Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

As shown in Figure 15 on page 9, depending on output current, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has reached the upper threshold of the PFM hysteretic, which is at 1.5% above the nominal output voltage. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold of the voltage hysteretic, which is the nominal output voltage. Then the PFM operation repeats.

Variable Peak Current Limit Scheme

To optimize efficiency across the output current range, the ISL9120IR implements a multi-level current limit scheme with 32 levels between 350mA and 2A. The transition from one level to the other is determined by the number of pulses in a PFM burst (pulse count) as shown in Figure 16. At a given peak current limit level, the pulse count increases as the output current increases. When the pulse count reaches the upper threshold at the existing current limit, the current limit will switch to the next higher level. Similarly, if the pulse count reaches the lower threshold at the existing current limit, the device will switch to the next lower level of peak current limit. If the pulse count reaches the upper threshold at the highest current limit, the current limit will not rise any further. Increasing the output current beyond this point may cause the output to lose voltage regulation.

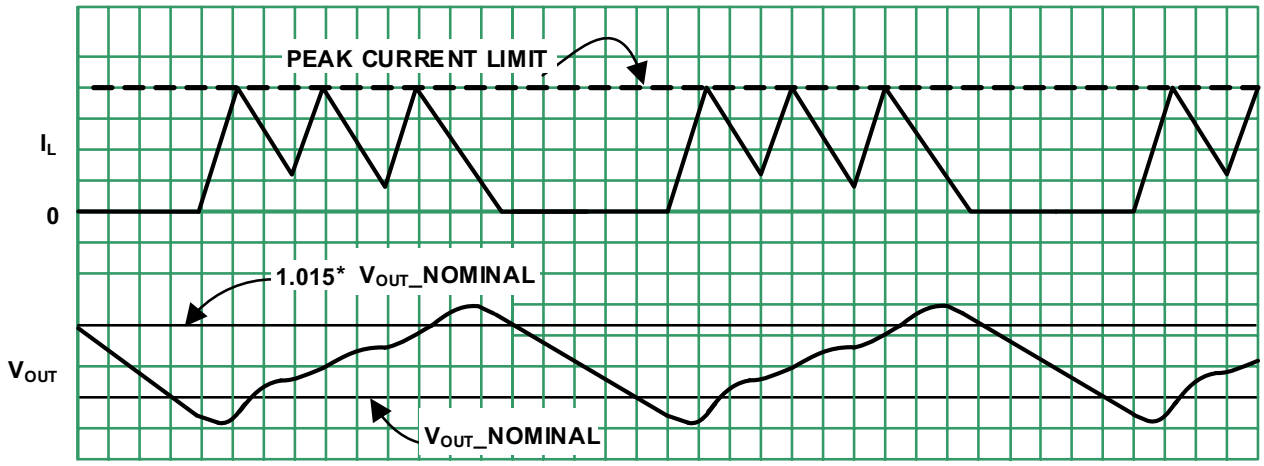


FIGURE 15. PFM MODE OPERATION CONCEPT

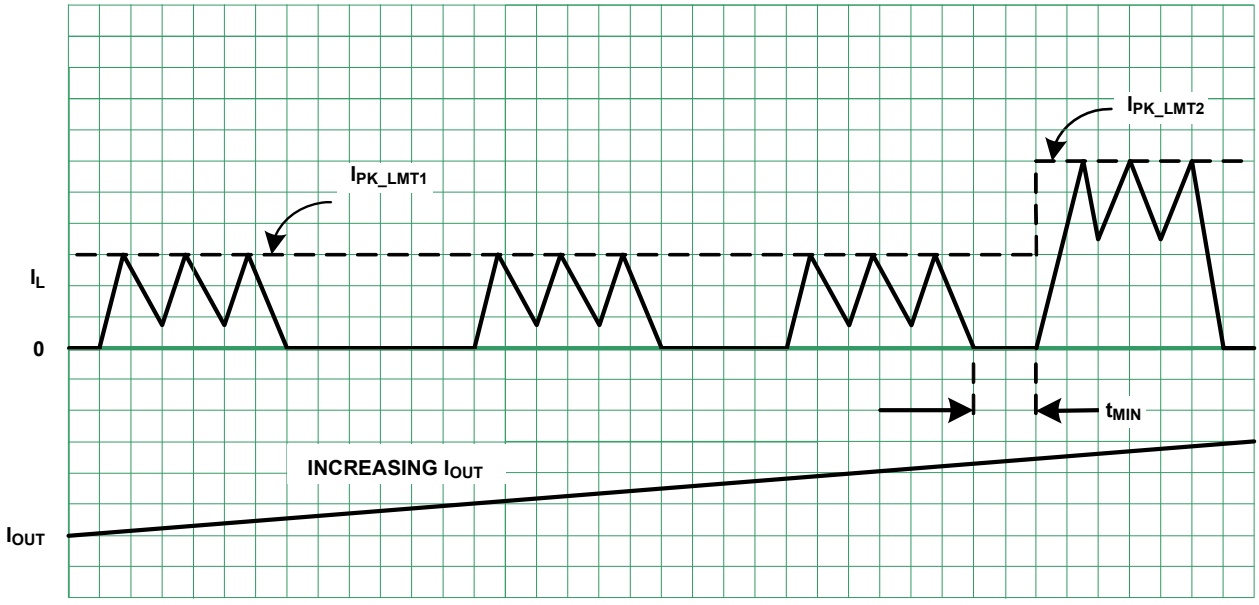


FIGURE 16. PEAK CURRENT LIMIT STEP UP TRANSITION

Automatic Bypass Mode Operation

When the output voltage is close to the input voltage, generally within 1% to 2%, the ISL9120IR will engage automatic bypass mode operation, which produces a direct connection between the VIN and VOUT pins. This behavior provides excellent efficiency and very low output voltage ripple.

Forced Bypass Mode Operation

Forced bypass mode operation is intended for applications where the output regulation is not important but the device quiescent current consumption is important. One example is when the buck-boost regulator is providing power to a LDO and the LDO is in standby mode with near zero output current. Under this condition, putting the buck-boost regulator in the bypass mode will have essentially no impact on the LDO but save the 41µA quiescent current consumption on the buck-boost regulator.

Since the bypass mode is an extreme power saving mode, there is no overcurrent protection. Therefore, caution must be taken not to overload or short-circuit the device. Power-up in the bypass mode is not recommended.

Output Voltage Programming

The ISL9120IR is available in fixed and adjustable output voltage versions. To use the fixed output version (ISL9120IRNZ), the VOUT pin must be connected directly to the FB pin.

In the adjustable output voltage version (ISL9120IRAZ), an external resistor divider is required to program the output voltage.

Applications Information

Component Selection

The fixed-output version (ISL9120IRNZ) requires only three external power components to implement the buck-boost converter: an inductor, an input capacitor and an output capacitor.

The adjustable version (ISL9120IRAZ) requires three additional components to program the output voltage. Two external resistors program the output voltage and a small capacitor is added to improve transient response.

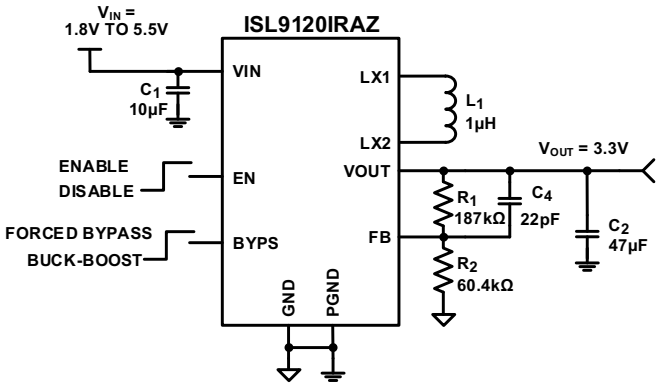


FIGURE 17. TYPICAL ISL9120IRAZ APPLICATION

Output Voltage Programming, Adjustable Version

Setting and controlling the output voltage of the ISL9120IRAZ (adjustable output version) can be accomplished by selecting the external resistor values.

Equation 1 can be used to derive the R_1 and R_2 resistor values:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

When designing a PCB, include a GND guard band around the FB resistor network to reduce noise and improve accuracy and stability. Resistors R_1 and R_2 should be positioned close to the FB pin. The suggested value of the R_1 resistor is 187k.

Feed-Forward Capacitor Selection

A small capacitor (C_4 in Figure 17) in parallel with resistor R_1 is required to provide the specified load and line regulation. The suggested value of this capacitor is 22pF for R_1 = 187k. An NPO type capacitor is recommended.

Non-Adjustable Version FB Pin Connection

The fixed output version of the ISL9120IR does not require external resistors or a capacitor on the FB pin. Simply connect VOUT to FB, as shown in Figure 18.

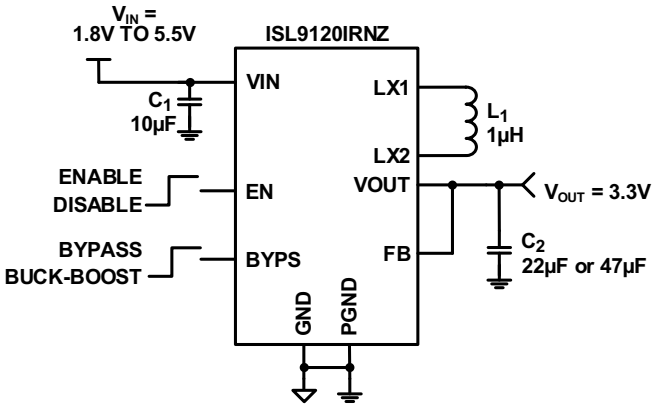


FIGURE 18. TYPICAL ISL9120IRNZAPPLICATION

Inductor Selection

An inductor with high frequency core material (e.g., ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with ≥2A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

TABLE 1. INDUCTOR VENDOR INFORMATION

MANUFACTURER	SERIES	DIMENSION (mm)	DCR (mΩ) TYP	I_{SAT} (A) TYP
Toko	DFE201610R-H-1R0M	2.0x1.6x1.0	66	2.7
Cyntec	PIFE20161T-1R0MS	2.0x1.6x1.0	65	2.8
TDK	TFM201610GHM-1R0MTAA	2.0x1.6x1.0	50	3.8

Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 10µF. The recommended 10µF input capacitor should have the following minimum characteristics: 0603 case size, X5R temperature range and 10V voltage rating. The recommended V_{OUT} capacitor values are 22µF or 47µF. The recommended 47µF output capacitor should have the following minimum characteristics: 0603 case size, X5R temperature range and 6.3V voltage rating. The recommended 22µF output capacitor should have the following minimum characteristics: 0603 case size, X5R temperature range and 10V voltage rating.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
TDK	X5R	www.tdk.com

Recommended PCB Layout

A correct PCB layout is critical for proper operation of the ISL9120IR. The input and output capacitors should be positioned as closely to the IC as possible. The ground connections of the input and output capacitors should be kept as short as possible and should be on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
February 2, 2016	FN8743.1	-page 1 - In “Description”, 3rd paragraph changed the value from 1µA to 3.5µA. -ordering information table on page 3, note1: Added “-T” suffix for 3k unit Tape and Reel options. -Analog specification table changes on page 4 are: Under power supply- VIN Undervoltage Lockout Threshold, changed max value from 1.775 to 1.79 VIN Supply Current, Bypass Mode changed Typ from 0.035 to 0.8 and max from 1 to 3.5. under output voltage regulation- Output Voltage Accuracy, changed Min/Max from -2 and +2 to -3 and +4.
August 4, 2015	FN8743.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

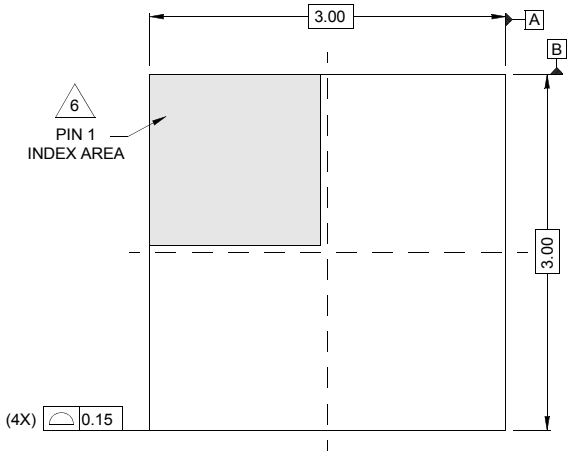
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

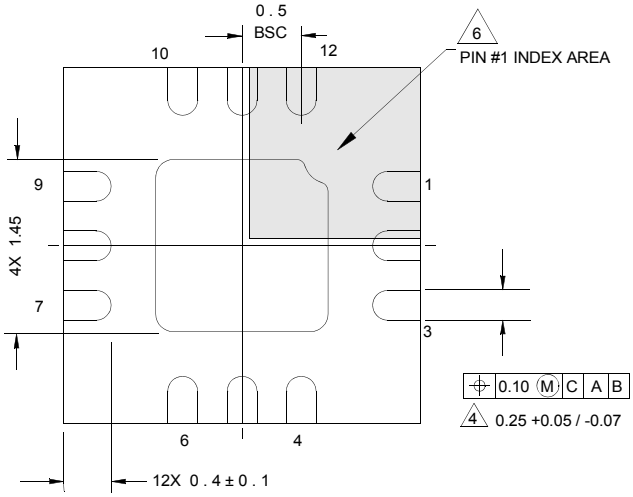
L12.3x3A

12 LEAD THIN QUAD FLAT NO LEAD PLASTIC PACKAGE

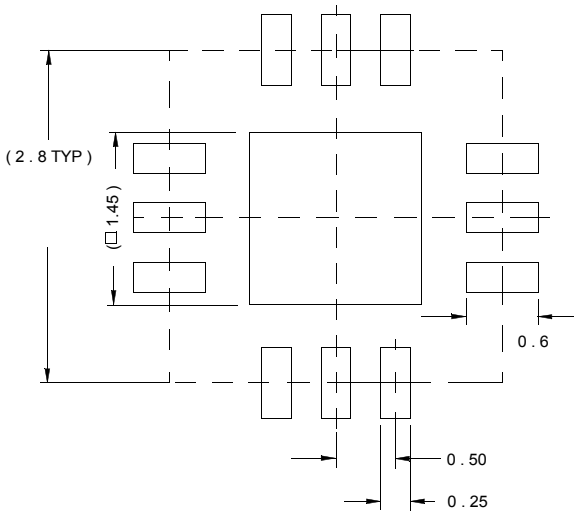
Rev 0, 09/07



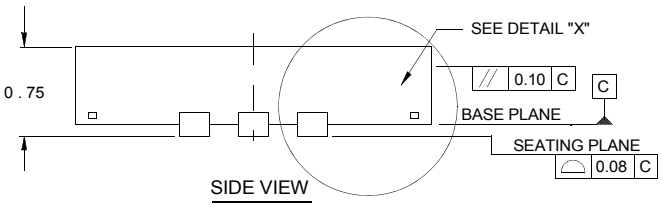
TOP VIEW



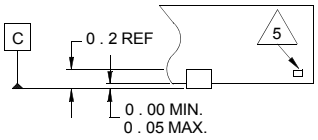
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.