The ISL85403 is a 40V, 2.5A synchronous buck or boost buck controller with a high-side MOSFET and low-side driver integrated. In buck mode, the ISL85403 supports a wide input range of 3V to 40V. In boost-buck mode, the input range can be extended down to 2.5V and output regulation can be maintained when VIN drops below VOUT, enabling sensitive electronics to remain on in low input voltage conditions.

The ISL85403 has a flexible selection of operation modes of forced PWM mode and PFM mode. In PFM mode, the quiescent input current is as low as 180µA (AUXVCC connected to VOUT). The load boundary between PFM and PWM can be programmed to cover wide applications.

The low-side driver can be either used to drive an external low-side MOSFET for a synchronous buck or left unused for a standard non-synchronous buck. The low-side driver can also be used to drive a boost converter as a preregulator followed by a buck controlled by the same IC, which greatly expands the operating input voltage range down to 2.5V or lower (Refer to “Typical Application Schematic III - Boost Buck Converter” on page 6).

The ISL85403 offers the most robust current protections. It uses peak current mode control with cycle-by-cycle current limiting. It is implemented with frequency foldback under current limit condition; also, the hiccup overcurrent mode is also implemented to guarantee reliable operations under harsh short conditions.

The ISL85403 has comprehensive protections against various faults including overvoltage and over-temperature protections, etc.

**Features**

- Buck mode: input voltage range 3V to 40V (refer to “Input Voltage” on page 15 for more details)
- Boost mode expands operating input voltage lower than 2.5V (refer to “Input Voltage” on page 15 for more details)
- Selectable forced PWM mode or PFM mode
- 300µA IC quiescent current (PFM, no load); 180µA input quiescent current (PFM, no load, VOUT tied to AUXVCC)
- Less than 5µA (MAX) shutdown input current (IC disabled)
- Operational topologies
  - Synchronous buck
  - Non-synchronous buck
  - Two-stage boost buck
  - Non-inverting single inductor buck boost
- Programmable frequency from 200kHz to 2.2MHz and frequency synchronization capability
- ±1% tight voltage regulation accuracy
- Reliable overcurrent protection
  - Temperature compensated current sense
  - Cycle-by-cycle current limiting with frequency foldback
  - Hiccup mode for worst case short condition
- 20 Ld 4x4 QFN package
- Pb-free (RoHS compliant)

**Applications**

- General purpose
- 24V bus power
- Battery power
- Point-of-load
- Embedded processor and I/O supplies

**Related Literature**

- AN1960, “ISL85403DEMO1Z Demonstration Board User Guide”
- UG010, “ISL85403EVAL2Z Evaluation Board User Guide”

---

**FIGURE 1. TYPICAL APPLICATION**

**FIGURE 2. EFFICIENCY, SYNCHRONOUS BUCK, PFM MODE, VOUT 5V, TA = +25°C**
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**Pin Configuration**

**ISL85403 (20 LD QFN)**

**TOP VIEW**

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>PIN #</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>1</td>
<td>The controller is enabled when this pin is left floating or pulled HIGH. The IC is disabled when this pin is pulled LOW. Range: 0V to 5.5V.</td>
</tr>
<tr>
<td>FS</td>
<td>2</td>
<td>Connecting this pin to VCC, or GND, or leaving it open will force the IC to have 500kHz switching frequency. The oscillator switching frequency can also be programmed by adjusting the resistor from this pin to GND.</td>
</tr>
<tr>
<td>SS</td>
<td>3</td>
<td>Connect a capacitor from this pin to ground. This capacitor, along with an internal 5µA current source, sets the soft-start interval of the converter. Also, this pin can be used to track a ramp on this pin.</td>
</tr>
<tr>
<td>FB</td>
<td>4</td>
<td>This pin is the inverting input of the voltage feedback error amplifier. With a properly selected resistor divider connected from $V_{OUT}$ to FB, the output voltage can be set to any voltage between the power rail (reduced by maximum duty cycle and voltage drop) and the 0.8V reference. Loop compensation is achieved by connecting an RC network across COMP and FB. The FB pin is also monitored for overvoltage events.</td>
</tr>
<tr>
<td>COMP</td>
<td>5</td>
<td>Output of the voltage feedback error amplifier.</td>
</tr>
<tr>
<td>ILIMIT</td>
<td>6</td>
<td>Programmable current limit pin. With this pin connected to the VCC pin, or to GND, or left open, the current limiting threshold is set to default of 3.6A; the current limiting threshold can be programmed with a resistor from this pin to GND.</td>
</tr>
<tr>
<td>MODE</td>
<td>7</td>
<td>Mode selection pin. Pull this pin to GND for forced PWM mode; to have it floating or connected to VCC will enable PFM mode when the peak inductor current is below the default threshold of 700mA. The current boundary threshold between PFM and PWM can also be programmed with a resistor at this pin to ground. Check for more details in the “PFM Mode Operation” on page 14.</td>
</tr>
<tr>
<td>PGOOD</td>
<td>8</td>
<td>PGOOD is an open-drain output and pull-up pin with a resistor to VCC for proper function. PGOOD will be pulled low under the events when the output is out of regulation (OV or UV) or EN pin is pulled low. PGOOD rising has a fixed 128 cycles delay.</td>
</tr>
<tr>
<td>PHASE</td>
<td>9, 10</td>
<td>These pins are the PHASE nodes that should be connected to the output inductor. These pins are connected to the source of the high-side N-channel MOSFET.</td>
</tr>
<tr>
<td>EXT(boost)</td>
<td>11</td>
<td>This pin is used to set boost mode and monitor the battery voltage that is the input of the boost converter. After $V_{CC}$ POR, the controller will detect the voltage on this pin; if voltage on this pin is below 200mV, the controller is set in synchronous/non-synchronous buck mode and will latch in this state unless $V_{CC}$ is below POR falling threshold; if the voltage on this pin after $V_{CC}$ POR is above 200mV, the controller is set in boost mode and latch in this state. In boost mode, the low-side driver output PWM with same duty cycle with upper-side driver to drive the boost switch. In boost mode, this pin is used to monitor input voltage through a resistor divider. By setting the resistor divider, the high threshold and hysteresis can be programmed. When voltage on this pin is above 0.8V, the PWM output (LGATE) for the boost converter is disabled, and when voltage on this pin is below 0.8V minus the hysteresis, the boost PWM is enabled.</td>
</tr>
</tbody>
</table>

**Functional Pin Descriptions**

In boost mode operation, PFM is disabled when boost PWM is enabled. Check the “2-Stage Boost Buck Converter Operation” on page 16 for more details.
SYNC 12 This pin can be used to synchronize two or more ISL85403 controllers. Multiple ISL85403s can be synchronized with their SYNC pins connected together. 180° phase shift is automatically generated between the master and slave ICs. The internal oscillator can also lock to an external frequency source applied on this pin with square pulse waveform (with frequency 10% higher than the IC's local frequency, and pulse width higher than 150ns). Range: 0V to 5.5V. This pin should be left floating if not used.

LGATE 13 In synchronous buck mode, this pin is used to drive the lower side MOSFET to improve efficiency. A 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise. In non-synchronous buck when a diode is used as the bottom side power device, this pin should be connected to VCC through a resistor (less than 5k) before IC start-up to have the low-side driver (LGATE) disabled. In boost mode, it can be used to drive the boost power MOSFET. The boost control PWM is same with the buck control PWM.

PGND 14 This pin is used as the ground connection of the power flow including driver. Connect it to large ground plane.

BOOT 15 This pin provides bias voltage to the high-side MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive the internal N-channel MOSFET. The boot charge circuitries are integrated inside of the IC. No external boot diode is needed. A 1µF ceramic capacitor is recommended to be used between BOOT and PHASE pin.

VIN 16, 17 Connect the input rail to these pins that are connected to the drain of the integrated high-side MOSFET as well as the source for the internal linear regulator that provides the bias of the IC. Range: 3V to 40V. With the part switching, the operating input voltage applied to the VIN pins must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to switching while not exceeding “Absolute Maximum Ratings” on page 7.

SGND 18 This pin provides the return path for the control and monitor portions of the IC. Connect it to a quiet ground plane.

VCC 19 This pin is the output of the internal linear regulator that supplies the bias for the IC including the driver. A minimum 4.7µF decoupling ceramic capacitor is recommended between VCC to ground.

AUXVCC 20 This pin is the input of the auxiliary internal linear regulator, which can be supplied by the regulator output after power-up. With such configuration, the power dissipation inside of the IC is reduced. The input range for this LDO is 3V to 20V. In boost mode operation, this pin works as boost output overvoltage detection pin. It detects the boost output through a resistor divider. When voltage on this pin is above 0.8V, the boost PWM is disabled; and when voltage on this pin is below 0.8V minus the hysteresis, the boost PWM is enabled. Range: 0V to 20V.

PAD - Bottom thermal pad. It is not connected to any electrical potential of the IC. In layout it must be connected to PCB ground copper plane with area as large as possible to effectively reduce the thermal impedance.

### Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER (Notes 1, 2, 3)</th>
<th>PART MARKING</th>
<th>TEMP. RANGE (°C)</th>
<th>PACKAGE (RoHS Compliant)</th>
<th>PKG. DWG. #</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISL85403FRZ</td>
<td>85 403FRZ</td>
<td>-40 to +105</td>
<td>20 Ld 4x4 QFN</td>
<td>L20.4x4C</td>
</tr>
<tr>
<td>ISL85403DEMO1Z</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL85403EVAL2Z</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL85403. For more information on MSL please see techbrief TB363.
Block Diagram

- Power-On Reset
- Bias LDO
- Auxiliary LDO
- Current Monitor
- Mode
- Oscillator
- Soft-Start Logic
- OPEN, OVP, OTP
- PFM Logic
- Boost Mode Control
- SLOPE Compensation
- Logic
- OSCILLATOR
- VIN
- PGND
- VIN (x2)
- SW
- FB
- COMP
- EA
- PGOOD
- PB
- SS
Typical Application Schematic I

(a) SYNCHRONOUS BUCK

(b) NON-SYNCHRONOUS BUCK

Typical Application Schematic II - VCC Switchover to VOUT

(a) SYNCHRONOUS BUCK

(b) NON-SYNCHRONOUS BUCK

Typical Application Schematic III - Boost Buck Converter

(a) 2-STAGE BOOST BUCK

(b) NON-INVERTING SINGLE INDUCTOR BUCK BOOST
**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min (Note 6)</th>
<th>Typ</th>
<th>Max (Note 6)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN Pin Supply</td>
<td>VIN Pin</td>
<td>VIN Pin</td>
<td>3.05</td>
<td>40</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Operating Supply Current</td>
<td>$I_Q$</td>
<td>MODE = VCC/FLOATING (PFM), no load at the output</td>
<td>300</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>$I_{IN_SD}$</td>
<td>EN connected to GND, $V_{IN}$ = 12V</td>
<td>2.8</td>
<td>4.5</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

**Thermal Information**

- **Thermal Resistance**
  - $\theta_{JA}$ ($^\circ$C/W): 40
  - $\theta_{JC}$ ($^\circ$C/W): 3.5

- **Maximum Junction Temperature**
  - Plastic Package: +150°C

- **Maximum Storage Temperature Range**:
  - -65°C to +150°C

**Recommended Operating Conditions**

- **Supply Voltage on $V_{IN}$**
  - 3V to 40V

- **$V_{AUXVCC}$**
  - GND - 0.3V to +20V

- **Ambient Temperature Range**
  - -40°C to +105°C

- **Junction Temperature Range**
  - -40°C to +125°C

**Electrical Specifications**

Refer to “Block Diagram” on page 5 and “Typical Application Schematics” on page 6. Operating Conditions Unless Otherwise Noted: $V_{IN}$ = 12V, or $V_{CC}$ = 4.5V ±10%, $T_A$ = -40°C to +105°C. Typicals are at $T_A$ = +25°C. Boldface limits apply across the operating temperature range, -40°C to +105°C.

**Notes:**

1. $T_A$ is measured in free air with the conformal coating and a single-sided heat sink.

2. $T_A$ is measured under free air conditions.

3. $T_A$ is measured under free air conditions with a single-sided heat sink.

4. $T_A$ is measured under free air conditions with a single-sided heat sink.

5. $T_A$ is measured under free air conditions with a single-sided heat sink.

**Electrical Specifications Table**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min (Note 6)</th>
<th>Typ</th>
<th>Max (Note 6)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN Pin Voltage Range</td>
<td>VIN</td>
<td>$V_{IN}$</td>
<td>3.05</td>
<td>40</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Operating Supply Current</td>
<td>$I_Q$</td>
<td>MODE = VCC/FLOATING (PFM), no load at the output</td>
<td>300</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>$I_{IN_SD}$</td>
<td>EN connected to GND, $V_{IN}$ = 12V</td>
<td>2.8</td>
<td>4.5</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

**INTERNAL MAIN LINEAR REGULATOR**

- **$V_{CC}$ Voltage**
  - $V_{IN} > 5V$ | 4.2 | 4.5 | 4.8 | V

- **$V_{DROP\_MAIN}$ Dropout Voltage**
  - $V_{IN} = 4.2V$, $I_{VCC}$ = 35mA | 0.3 | 0.52 | V
  - $V_{IN} = 3V$, $I_{VCC}$ = 35mA | 0.25 | 0.42 | V

- **$V_{CC}$ Current Limit of MAIN LDO**
  - 60 | mA

**INTERNAL AUXILIARY LINEAR REGULATOR**

- **$V_{AUXVCC}$ Input Voltage Range**
  - 3 | 20 | V

- **$V_{CC}$ Voltage**
  - $V_{AUXVCC} > 5V$ | 4.2 | 4.5 | 4.8 | V

- **$V_{DROP\_AUX}$ Dropout Voltage**
  - $V_{AUXVCC} = 4.2V$, $I_{VCC} = 35mA$ | 0.3 | 0.52 | V
  - $V_{AUXVCC} = 3V$, $I_{VCC} = 35mA$ | 0.25 | 0.42 | V

- **Current Limit of AUX LDO**
  - 60 | mA

- **AUX LDO Switchover Rising Threshold**
  - $V_{AUXVCC\_RISE}$ | AUXVCC voltage rise; Switch to auxiliary LDO | 2.97 | 3.1 | 3.2 | V

- **AUX LDO Switchover Falling Threshold Voltage**
  - $V_{AUXVCC\_FALL}$ | AUXVCC voltage fall; Switch back to main BIAS LDO | 2.73 | 2.87 | 2.97 | V

- **AUX LDO Switchover Hysteresis**
  - $V_{AUXVCC\_HYS}$ | AUXVCC switchover hysteresis | 0.2 | V
## Electrical Specifications

Refer to “Block Diagram” on page 5 and “Typical Application Schematics” on page 6. Operating Conditions Unless Otherwise Noted: \( V_{IN} = 12\,V, \) or \( V_{CC} = 4.5\,V \pm10\%, \) \( T_A = -40^\circ C \) to \(+105^\circ C\). Typicals are at \( T_A = +25^\circ C\). Boldface limits apply across the operating temperature range, \(-40^\circ C \) to \(+105^\circ C\). (Continued)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN (Note 6)</th>
<th>TYP</th>
<th>MAX (Note 6)</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER-ON RESET</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rising ( V_{CC} ) POR Threshold</td>
<td>( V_{PORH_RISE} )</td>
<td></td>
<td>2.82</td>
<td>2.9</td>
<td>3.05</td>
<td>V</td>
</tr>
<tr>
<td>Falling ( V_{CC} ) POR Threshold</td>
<td>( V_{PORL_FALL} )</td>
<td></td>
<td>2.6</td>
<td>2.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{CC} ) POR Hysteresis</td>
<td>( V_{PORL_HYS} )</td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>ENABLE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable On Voltage</td>
<td>( V_{ENH} )</td>
<td></td>
<td>1.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Enable Off voltage</td>
<td>( V_{ENL} )</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>EN Pull-up Current</td>
<td>( I_{EN_PULLUP} )</td>
<td>( V_{EN} = 1.2V, V_{IN} = 24V )</td>
<td>1.5</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{EN} = 1.2V, V_{IN} = 12V )</td>
<td>1.2</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{EN} = 1.2V, V_{IN} = 5V )</td>
<td>0.9</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td><strong>OSCILLATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWM Frequency</td>
<td>( F_{OSC} )</td>
<td>( R_T = 665k\Omega )</td>
<td>160</td>
<td>200</td>
<td>240</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_T = 51.1k\Omega )</td>
<td>1870</td>
<td>2200</td>
<td>2530</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FS pin connected to ( V_{CC} ) or floating or GND</td>
<td>450</td>
<td>500</td>
<td>550</td>
<td>kHz</td>
</tr>
<tr>
<td>MIN ON Time</td>
<td>( t_{MIN_ON} )</td>
<td></td>
<td>130</td>
<td></td>
<td>225</td>
<td>ns</td>
</tr>
<tr>
<td>MIN OFF Time</td>
<td>( t_{MIN_OFF} )</td>
<td></td>
<td>210</td>
<td></td>
<td>330</td>
<td>ns</td>
</tr>
<tr>
<td><strong>SYNCHRONIZATION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input High Threshold</td>
<td>( V_{IH} )</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Low Threshold</td>
<td>( V_{IL} )</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Minimum Pulse Width</td>
<td></td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Input Impedance</td>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>( k\Omega )</td>
</tr>
<tr>
<td>Input Minimum Frequency Divided by Free Running Frequency</td>
<td></td>
<td></td>
<td>1.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Maximum Frequency Divided by Free Running Frequency</td>
<td></td>
<td></td>
<td>1.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Pulse Width</td>
<td></td>
<td>( C_{SYNC} = 100pF )</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Output Pulse High</td>
<td>( V_{OH} )</td>
<td>( R_{LOAD} = 1k\Omega )</td>
<td>VCC-0.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Pulse Low</td>
<td>( V_{OL} )</td>
<td></td>
<td>GND</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>REFERENCE VOLTAGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Voltage</td>
<td>( V_{REF} )</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>System Accuracy</td>
<td></td>
<td></td>
<td>(-1.0)</td>
<td></td>
<td>(+1.0)</td>
<td>%</td>
</tr>
<tr>
<td>FB Pin Source Current</td>
<td></td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Soft-start</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Soft-start Current</td>
<td>( I_{SS} )</td>
<td></td>
<td>3</td>
<td>5</td>
<td>7</td>
<td>( \mu A )</td>
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<tr>
<td><strong>ERROR AMPLIFIER</strong></td>
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<tr>
<td>Unity Gain-bandwidth</td>
<td>( C_{LOAD} = 50pF )</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>MHz</td>
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<tr>
<td>DC Gain</td>
<td>( C_{LOAD} = 50pF )</td>
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<td>88</td>
<td></td>
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<td>Maximum Output Voltage</td>
<td></td>
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<td>3.6</td>
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<td></td>
<td>V</td>
</tr>
<tr>
<td>Minimum Output Voltage</td>
<td></td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>( SR )</td>
<td>( C_{LOAD} = 50pF )</td>
<td>5</td>
<td></td>
<td></td>
<td>V/\mu s</td>
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FN8631 Rev 1.00
March 13, 2015

**RENAESAS**
### Electrical Specifications

Refer to "Block Diagram" on page 5 and "Typical Application Schematics" on page 6. Operating Conditions

Unless Otherwise Noted: $V_{IN} = 12V$, or $V_{CC} = 4.5V \pm 10\%$, $T_A = -40^\circ C$ to $+105^\circ C$. Typicals are at $T_A = +25^\circ C$. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN (Note 6)</th>
<th>TYP</th>
<th>MAX (Note 6)</th>
<th>UNITS</th>
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<tbody>
<tr>
<td><strong>PFM MODE CONTROL</strong></td>
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<tr>
<td>Default PFM Current Threshold</td>
<td>MODE = VCC or floating</td>
<td></td>
<td>700</td>
<td>mA</td>
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<td><strong>INTERNAL HIGH-SIDE MOSFET</strong></td>
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<tr>
<td>Upper MOSFET $r_{DS(ON)}$</td>
<td>$r_{DS(ON)_UP}$</td>
<td>Limits apply for $+25^\circ C$ only</td>
<td>127</td>
<td>mΩ</td>
<td>140</td>
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<td><strong>LOW-SIDE MOSFET GATE DRIVER</strong></td>
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<td>LGate Source Resistance</td>
<td>100mA source current</td>
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<td>3.5</td>
<td>Ω</td>
<td></td>
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<tr>
<td>LGATE Sink Resistance</td>
<td>100mA sink current</td>
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<td>2.8</td>
<td>Ω</td>
<td></td>
<td></td>
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<tr>
<td><strong>BOOST CONVERTER CONTROL</strong></td>
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<tr>
<td>EXT_BOOST Boost_Off Threshold Voltage</td>
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<td>0.74</td>
<td>V</td>
<td>0.8</td>
<td>0.86</td>
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<td>EXT_BOOST Hysteresis Sink Current</td>
<td>$I_{EXT_BOOST_HYS}$</td>
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<td>2.1</td>
<td>μA</td>
<td>3.2</td>
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<tr>
<td>AUXVCC Boost Turn-Off Threshold Voltage</td>
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<td></td>
<td>0.74</td>
<td>V</td>
<td>0.8</td>
<td>0.86</td>
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<tr>
<td>AUXVCC Hysteresis Sink Current</td>
<td>$I_{AUXVCC_HYS}$</td>
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<td>2.1</td>
<td>μA</td>
<td>3.2</td>
<td>4.2</td>
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<tr>
<td><strong>POWER-GOOD MONITOR</strong></td>
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<tr>
<td>Overvoltage Rising Trip Point</td>
<td>$V_{FB}/V_{REF}$</td>
<td>Percentage of reference point</td>
<td>104</td>
<td>%</td>
<td>110</td>
<td>116</td>
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<tr>
<td>Overvoltage Rising Hysteresis</td>
<td>$V_{FB}/V_{OVTRIP}$</td>
<td>Percentage below OV trip point</td>
<td>3</td>
<td>%</td>
<td></td>
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<tr>
<td>Undervoltage Falling Trip Point</td>
<td>$V_{FB}/V_{REF}$</td>
<td>Percentage of reference point</td>
<td>84</td>
<td>%</td>
<td>90</td>
<td>96</td>
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<tr>
<td>Undervoltage Falling Hysteresis</td>
<td>$V_{FB}/V_{UVTRIP}$</td>
<td>Percentage above UV trip point</td>
<td>3</td>
<td>%</td>
<td></td>
<td></td>
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<td>PGOOD Rising Delay</td>
<td>$t_{PGOOD_R_DELAY}$</td>
<td></td>
<td>128</td>
<td>cycle</td>
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<tr>
<td>PGOOD Leakage Current</td>
<td>PGOOD HIGH, $V_{PGOOD} = 4.5V$</td>
<td></td>
<td>10</td>
<td>nA</td>
<td></td>
<td></td>
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<tr>
<td>PGOOD Low Voltage</td>
<td>$V_{PGOOD}$</td>
<td>PGOOD LOW, $I_{PGOOD} = 0.2mA$</td>
<td>0.10</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td><strong>OVERCURRENT PROTECTION</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Default Cycle-by-cycle Current Limit Threshold</td>
<td>$I_{OC_1}$</td>
<td>$I_{LIMIT} = GND or VCC or floating</td>
<td>3</td>
<td>A</td>
<td>3.6</td>
<td>4.2</td>
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<tr>
<td>Hiccup Current Limit Threshold</td>
<td>$I_{OC_2}$</td>
<td>Hiccup, $I_{OC_2}/I_{OC_1}$</td>
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<td>%</td>
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<tr>
<td><strong>OVERRANGE PROTECTION</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OV 120% Trip Point</td>
<td>$V_{FB}/V_{REF}$</td>
<td>Active in and after soft-start. Percentage of reference point $LG = UG = LOW$</td>
<td>120</td>
<td>%</td>
<td></td>
<td></td>
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<tr>
<td>OV 120% Release Point</td>
<td>$V_{FB}/V_{OVTRIP}$</td>
<td>Active in and after soft-start. Percentage of reference point</td>
<td>102.5</td>
<td>%</td>
<td></td>
<td></td>
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<tr>
<td>OV 110% Trip Point</td>
<td>$V_{FB}/V_{REF}$</td>
<td>Active after soft-start done. Percentage of reference point $LG = UG = LOW$</td>
<td>110</td>
<td>%</td>
<td></td>
<td></td>
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<tr>
<td>OV 110% Release Point</td>
<td>$V_{FB}/V_{UVTRIP}$</td>
<td>Active after soft-start done. Percentage of reference point</td>
<td>102.5</td>
<td>%</td>
<td></td>
<td></td>
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<tr>
<td><strong>OVER-TEMPERATURE PROTECTION</strong></td>
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<tr>
<td>Over-temperature Trip Point</td>
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<td>°C</td>
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<tr>
<td>Over-temperature Recovery Threshold</td>
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<td></td>
<td>140</td>
<td>°C</td>
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<td></td>
</tr>
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</table>

**NOTE:**

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
**Typical Performance Curves**

**FIGURE 3. EFFICIENCY, SYNCHRONOUS BUCK, FORCED PWM MODE, 500kHz, VOUT 5V, TA = +25°C**

**FIGURE 4. EFFICIENCY, SYNCHRONOUS BUCK, PFM MODE, VOUT 5V, TA = +25°C**

**FIGURE 5. LINE REGULATION, VOUT 5V, TA = +25°C**

**FIGURE 6. LOAD REGULATION, VOUT 5V, TA = +25°C**

**FIGURE 7. EFFICIENCY, SYNCHRONOUS BUCK, FORCED PWM MODE, 500kHz, VOUT 3.3V, TA = +25°C**

**FIGURE 8. EFFICIENCY, SYNCHRONOUS BUCK, PFM MODE, VOUT 3.3V, TA = +25°C**
Typical Performance Curves (Continued)

FIGURE 9. INPUT QUIESCENT CURRENT UNDER NO LOAD, PFM MODE, $V_{OUT} = 5V$

FIGURE 10. SYNCHRONOUS BUCK MODE, $V_{IN} 36V, I_O 2A$, ENABLE ON

FIGURE 11. SYNCHRONOUS BUCK MODE, $V_{IN} 36V, I_O 2A$, ENABLE OFF

FIGURE 12. $V_{IN} 36V$, PREBIASED START-UP

FIGURE 13. SYNCHRONOUS BUCK WITH FORCE PWM MODE, $V_{IN} 36V, I_O 2A$

FIGURE 14. $V_{IN} 24V$, 0 TO 2A STEP LOAD, FORCE PWM MODE
Typical Performance Curves (Continued)

FIGURE 15. $V_{IN} 24V$, 80mA LOAD, PFM MODE

FIGURE 16. $V_{IN} 24V$, 0 TO 2A STEP LOAD, PFM MODE

FIGURE 17. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, $V_{IN} 12V$, NO LOAD

FIGURE 18. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, $V_{IN} 12V$, 2A

FIGURE 19. BOOST BUCK MODE, BOOST INPUT STEP FROM 36V TO 3V, $V_{OUT} BUCK = 5V$, $I_{OUT_BUCK} = 1A$

FIGURE 20. BOOST BUCK MODE, BOOST INPUT STEP FROM 3V TO 36V, $V_{OUT} BUCK = 5V$, $I_{OUT_BUCK} = 1A$
Typical Performance Curves (Continued)

**FIGURE 21.** BOOST BUCK MODE, $V_O = 9V$, $I_O = 1.8A$, BOOST INPUT DROPS FROM 16V TO 9V DC

**FIGURE 22.** EFFICIENCY, BOOST BUCK, 500kHz, $V_{OUT} 12V$, $T_A = +25^\circ C$

**FIGURE 23.** UPPER MOSFET $r_{DS(ON)}$ (mΩ) OVER-TEMPERATURE
Functional Description

Initialization
Initially the ISL85403 continually monitors the voltage at the EN pin. When the voltage on the EN pin exceeds its rising ON threshold, the internal LDO will start-up to build up VCC. After Power-on Reset (POR) circuits detect that VCC voltage has exceeded the POR threshold, the soft-start will be initiated.

Soft-start
The soft-start (SS) ramp is built up in the external capacitor on the SS pin that is charged by an internal 5µA current source.

\[ C_{SS}[\mu F] = 6.5 \cdot t_{SS}[S] \]  

(EQ. 1)

The SS ramp starts from 0 to a voltage above 0.8V. Once SS reaches 0.8V, the bandgap reference takes over and IC gets into steady state operation. The soft-start time is referring to the duration for SS pin ramps from 0 to 0.8V while output voltage ramps up with the same rate from 0 to target regulated voltage. The required capacitance at SS pin can be calculated from Equation 1.

The SS plays a vital role in the hiccup mode of operation. The IC works as cycle-by-cycle peak current limiting at overload condition. When a harsh condition occurs and the current in the upper side MOSFET reaches the second overcurrent threshold, the SS pin is pulled to ground and a dummy soft-start cycle is initiated. At dummy SS cycle, the current to charge soft-start capacitor is cut down to 1/5 of its normal value. Thus, a dummy SS cycle takes 5x of the regular SS cycle. During the dummy SS period, the control loop is disabled and no PWM output. At the end of this cycle, it will start the normal SS. The hiccup mode persists until the second overcurrent threshold is no longer reached.

The ISL85403 is capable of starting up with prebiased output.

PWM Control
Pulling the MODE pin to GND will set the IC in forced PWM mode. The ISL85403 employs the peak current mode PWM control for fast transient response and cycle-by-cycle current limiting. See "Block Diagram" on page 5.

The PWM operation is initialized by the clock from the oscillator. The upper MOSFET is turned on by the clock at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current sense signal and the slope compensation signal reaches the error amplifier output voltage level, the PWM comparator is triggered to shut down the PWM logic to turn off the high-side MOSFET. The high-side MOSFET stays off until the next clock signal comes for next cycle.

The output voltage is sensed by a resistor divider from VOUT to the FB pin. The difference between the FB voltage and 0.8V reference is amplified and compensated to generate the error voltage signal at the COMP pin. Then the COMP pin signal is compared with the current ramp signal to shut down the PWM.

PFM Mode Operation
To pull the MODE pin HIGH (>2.5V) or leave the MODE pin floating will set the IC to have PFM (Pulse Frequency Modulation) operation in light load. In PFM mode, the switching frequency is dramatically reduced to minimize the switching loss. The ISL85403 enters PFM mode when the MOSFET peak current is lower than the PWM/PFM boundary current threshold. The default threshold is 700mA when there is no programming resistor at the MODE pin.

The current threshold for PWM/PFM boundary can be programmed by choosing the MODE pin resistor value calculated from Equation 2.

\[ R_{MODE} = \frac{118500}{I_{PFM} + 0.2} \]  

(EQ. 2)

where \( I_{PFM} \) is the desired PWM/PFM boundary current threshold and \( R_{MODE} \) is the programming resistor. The usable resistor value range to program PFM current threshold is 150kΩ to 200kΩ. \( R_{MODE} \) value out of this range is not recommended.

Synchronous and Non-Synchronous Buck
The ISL85403 supports both Synchronous and non-synchronous buck operations.

In synchronous buck configuration, a 5.1k or smaller value resistor must be added from LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise.

For a non-synchronous buck operation when a power diode is used as the low-side power device, the LGATE driver can be disabled with LGATE connected to VCC (before IC start-up). For non-synchronous buck, the phase node will show oscillations after high-side turns off (as shown in Figure 17 on page 12 - blue trace). This is normal due to the oscillations among the parasitic capacitors at phase node and output inductor. A RC snubber (suggesting 200Ω and 2.2nF as typical) at phase node can reduce this ringing.
AUXVCC Switchover

The ISL85403 has an auxiliary LDO integrated as shown in the “Block Diagram” on page 5. It is used to replace the internal MAIN LDO function after the IC start-up. “Typical Application Schematic II - VCC Switchover to VOUT” on page 6 shows its basic application setup with output voltage connected to AUXVCC. After IC soft-start is done and the output voltage is built up to steady state, and once the AUXVCC pin voltage is over the AUX LDO Switchover Rising Threshold, the MAIN LDO is shut off and the AUXILIARY LDO is activated to bias VCC. Since the AUXVCC pin voltage is lower than the input voltage VIN, the internal LDO dropout voltage and the consequent power loss is reduced. This feature brings substantial efficiency improvements in light load range, especially at high input voltage applications.

When the voltage at AUXVCC falls below the AUX LDO Switchover Falling Threshold, the AUXILIARY LDO is shut off and the MAIN LDO is reactivated to bias VCC. At the OV/UV fault events, the IC also switches back over from AUXILIARY LDO to MAIN LDO.

The AUXVCC switchover function is offered in buck configuration. It is not offered in boost configuration when the AUXVCC pin is used to monitor the boost output voltage for OVP.

Input Voltage

With the part switching, the operating ISL85403 input voltage must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to part switching while not exceeding the 44V, as stated in the Absolute Maximum Ratings.

The lowest IC operating input voltage (VIN pin) depends on VCC voltage and the Rising and Falling VCC POR Threshold in Electrical Specifications table on page 8. At IC start-up when VCC is just over rising POR threshold, there is no switching before the soft-start starts. Therefore, the IC minimum start-up voltage on the VIN pin is 3.05V (MAX of Rising VCC POR). When the soft-start is initiated, the regulator is switching and the dropout voltage across the internal LDO increases due to driving current. Thus, the IC VIN pin shutdown voltage is related to driving current and VCC POR falling threshold. The internal upper side MOSFET has typical 10nC gate drive. For a typical example of synchronous buck with 4nC lower MOSFET gate drive and 500kHz switching frequency, the driving current is 7mA total causing 70mV drop across internal LDO under 3V VIN. Then the IC shutdown voltage on the VIN pin is 2.87V (2.8V + 0.07V). In practical design, extra room should be taken into account with concern to voltage spikes at VIN.

With boost buck configuration, the input voltage range can be expanded further down to 2.5V or lower depending on the boost stage voltage drop upon maximum duty cycle. Since the boost output voltage is connected to the VIN pin as the buck inputs, after the IC starts up, the IC will keep operating and switching as long as the boost output voltage can keep the VCC voltage higher than the falling threshold. Refer to “2-Stage Boost Buck Converter Operation” on page 16 for more details.

Output Voltage

The output voltage can be programmed down to 0.8V by a resistor divider from VOUT to FB. For Buck, the maximum achievable voltage is (VIN*D_MAX - VDROP), where VDROP is the voltage drop in the power path including mainly the MOSFET rDS(ON) and inductor DCR. The maximum duty cycle D_MAX is decided by (1 - fSW * tMIN(OFF)).

Output Current

With the high-side MOSFET integrated, the maximum output current, which the ISL85403 can support is decided by the package and many operating conditions including input voltage, output voltage, duty cycle, switching frequency and temperature, etc. From the thermal perspective, the die temperature shouldn’t exceed +125°C with the power loss dissipated inside of the IC.

Note that more temperature rise is expected at higher ambient temperature due to more conduction loss caused by fDS(ON) increase.

Basically, the die temperature is equal to the sum of ambient temperature and the temperature rise resulting from the power dissipated by the IC package with a certain junction to ambient thermal impedance θJA. The power dissipated in the IC is related to the MOSFET switching loss, conduction loss and the internal LDO loss. Besides the load, these losses are also related to input voltage, output voltage, duty cycle, switching frequency and temperature. With the exposed pad at the bottom, the heat of the IC mainly goes through the bottom pad and θJA is greatly reduced. The θJA is highly related to layout and air flow conditions. In layout, multiple vias (≥9) are strongly recommended in the IC bottom pad. The bottom pad with its vias should be placed in the ground copper plane with an area as large as possible across multiple layers. The θJA can be reduced further with air flow. Refer to Figures 8 and 9 for the thermal performance with 100 CFM air flow.

For applications with high output current and bad operating conditions (compact board size, high ambient temperature, etc.), synchronous buck is highly recommended since the external low-side MOSFET generates smaller heat than external low-side power diode. This helps to reduce PCB temperature rise around the ISL85403 and less junction temperature rise.
2-Stage Boost Buck Converter Operation

The “Typical Application Schematic III - Boost Buck Converter” on page 6, shows the circuits of boost function. Schematic (a) shows a boost working as a pre-stage to provide input to the following Buck stage. This is for applications when the input voltage could drop to a very low voltage in some constants (i.e., in some battery powered systems), causing the output voltage to drop out of regulation. The boost converter can be enabled to boost the input voltage up to keep the output voltage in regulation. When system input voltage recovers back to normal, the boost stage is disabled while only the buck stage is switching.

The EXT_BOOST pin is used to set boost mode and monitor the boost input voltage. At IC start-up before soft-start, the controller will be latched in boost mode when the voltage is at or above 200mV; it will latch in synchronous buck mode if voltage on this pin is below 200mV. In boost mode, the low-side driver output PWM has the same PWM signal with the buck regulator.

In boost mode, the EXT_BOOST pin is used to monitor boost input voltage to turn on and turn off the boost PWM. The AUXVCC pin is used to monitor the boost output voltage to turn on and turn off the boost PWM.

Referring to Figure 25, a resistor divider from boost input voltage to the EXT_BOOST pin is used to detect the boost input voltage. When the voltage on EXT_BOOST pin is below 0.8V, the boost PWM is enabled with a fixed 500µs soft-start and the boost duty cycle increases linearly from t_MIN(ON)*Fs to ~50%. A 3µA sinking current is enabled at the EXT_BOOST pin for hysteresis purposes. When the voltage on the EXT_BOOST pin recovers to be above 0.8V, the boost PWM is disabled immediately. Use Equation 3 to calculate the upper resistor R_UP (R1 in Figure 25) for a desired hysteresis VHYS at boost input voltage.

\[ R_{UP} = \frac{V_{HYS}}{3 \mu A} \]  

(EQ. 3)

Use Equation 4 to calculate the lower resistor R_LOW (R2 in Figure 25) according to a desired boost enable threshold.

\[ R_{LOW} = \frac{R_{UP} \cdot 0.8}{V_{FTH} - 0.8} \]  

(EQ. 4)

Where VFTH is the desired falling threshold on boost input voltage to turn on the boost, 3µA is the hysteresis current and 0.8V is the reference voltage to be compared with.

Note that the boost start-up threshold has to be selected in a way that the buck is operating working well and kept in close loop regulation before boost start-up. Otherwise, large inrush current at boost start-up could occur at boost input due to the buck open loop saturation. The boost start-up input voltage threshold should be set high enough to cover the DC voltage drop of boost inductor and diode, also the buck’s maximum duty cycle and voltage conduction drop. This ensures buck is not reaching maximum duty cycle before boost start-up.

Similarly, a resistor divider from the boost output voltage to the AUXVCC pin is used to detect the boost output voltage. When the voltage on the AUXVCC pin is below 0.8V, the boost PWM is enabled with a fixed 500µs soft-start and a 3µA sinking current is enabled at AUXVCC pin for hysteresis purposes. When the voltage on the AUXVCC pin recovers to be above 0.8V, the boost PWM is disabled immediately. Use Equation 3 to calculate the upper resistor R_UP (R3 in Figure 25) according to a desired hysteresis V_HYS at boost output voltage. Use Equation 4 to calculate the lower resistor R_LOW (R4 in Figure 25) according to a desired boost enable threshold at boost output.

Assuming V_BAT is the boost input voltage, V_OUT_BST is the boost output voltage and V_OUT is the buck output voltage, the steady state DC transfer function are:

\[ V_{OUTBST} = \frac{1}{1 - D} \cdot V_{BAT} \]  

(EQ. 5)

\[ V_{OUT} = D \cdot V_{OUTBST} = \frac{D}{1 - D} \cdot V_{BAT} \]  

(EQ. 6)
From Equations 5 and 6, Equation 7 can be derived to estimate the steady state boost output voltage as function of \( V_{BAT} \) and \( V_{OUT} \):

\[
V_{OUTBST} = V_{BAT} + V_{OUT}
\]  
\[
(EQ. \ 7)
\]

After the IC starts up, the boost buck converters can keep working when the battery voltage drops extremely low because the IC’s bias (VCC) LDO is powered by the boost output. For example, a 3.3V output application battery drops to 2V, and the VIN pin voltage is powered by the boost output voltage that is 5.2V (Equation 7), meaning that the VIN pin (boost input) still sees 5.2V to keep the IC working.

Note that in the previously mentioned case, the boost input current could be high because the input voltage is very low (\( V_{IN} = V_{OUT}/\text{Efficiency} \)). If the design is to achieve the low input operation with full load, the inductor and MOSFET have to be selected with enough current ratings to handle the high current appearing at boost input. The boost inductor current are the same with the boost input current, which can be estimated as Equation 8, where \( P_{OUT} \) is the output power, \( V_{BAT} \) is the boost input voltage, and EFF is the estimated efficiency of the whole boost and buck stages.

\[
I_{LIN} = \frac{P_{OUT}}{V_{BAT} \cdot \text{EFF}}
\]  
\[
(EQ. \ 8)
\]

Based on the same concerns of boost input current, the start-up sequence must follow the rule that the IC is enabled after the boost input voltage rise above a certain level. The shutdown sequence must follow the rule that the IC is disabled first before the boost input power source is turned off. At boost mode applications where there is no external control signal to enable/disable the IC, an external input UVLO circuit must be implemented for the start-up and shutdown sequence.

### Non-Inverting Single Inductor Buck Boost Converter Operation

In “Typical Application Schematic III - Boost Buck Converter” on page 6, schematic (b) shows non-inverting single inductor buck boost configuration. The recommended setting is to use resistor divider 1MΩ and 130kΩ (as shown in TYP Schematic III b) connecting from VCC to both EXT_BOOST and AUXVCC pins (EXT_BOOST and AUXVCC pin are directly connected). In this way, the EXT_BOOST pin voltage is a fixed voltage 0.52V that is higher than the boost mode detection threshold 0.2V to set IC in boost mode and lower than the boost switching threshold 800mV to have boost being constantly switching (during and after soft-start).

As the same in 2-stage boost buck mode, LGATE is switching ON with the same phase of upper FETs switching ON, meaning both upper and lower side FETs are ON and OFF at the same time with the same duty cycle. When both FETs are ON, input voltage charges inductor current ramping up for duration of DT; when both FETs are OFF, inductor current is free wheeling through the 2 power diodes to output and output voltage discharge the inductor current ramping down for (1-D)T (in CCM mode). The steady state DC transfer function is:

\[
V_{OUT} = \frac{D}{1-D} V_{IN}
\]  
\[
(EQ. \ 9)
\]

Where \( V_{IN} \) is the input voltage, \( V_{OUT} \) is the boost buck output voltage, D is duty cycle.

**Equation 10** is another useful equation used to calculate the inductor DC current as below:

\[
I_{LDC} = \frac{1}{1-D} I_{OUT}
\]  
\[
(EQ. \ 10)
\]

Where \( I_{LDC} \) is the inductor DC current and \( I_{OUT} \) is the output DC current.

**Equation 10** shows the inductor current is charging output only during (1-D)T, which means inductor current has less load current capability compared with buck and 2-stage boost buck configurations. Its load current capability depends mainly on the duty cycle and inductor current.

Inductor ripple current can be calculated using **Equation 11**:

\[
I_{LPRK} = \frac{V_{OUT}(1-D)T}{L}
\]  
\[
(EQ. \ 11)
\]

The inductor peak current is,

\[
I_{LPEAK} = I_{LDC} + \frac{1}{2} I_{LPRK}
\]  
\[
(EQ. \ 12)
\]

In power stage DC calculations, use **Equation 9** to calculate D, then use **Equation 10** to calculate \( I_{LDC} \). D and \( I_{LDC} \) are useful information to estimate the high-side FET’s power losses and check if the part can meet the load current requirements.

### Oscillator and Synchronization

The oscillator has a default frequency of 500kHz with the FS pin connected to VCC, or ground, or floating. The frequency can be programmed to any frequency between 200kHz and 2.2MHz with a resistor from FS pin to GND.

\[
R_{FS} \quad [\Omega] = \frac{145000 - 16 \cdot f_{SW}[kHz]}{f_{SW}[kHz]}
\]  
\[
(EQ. \ 13)
\]

**FIGURE 26.** \( R_{FS} \) vs FREQUENCY

The SYNC pin is bidirectional and it outputs the IC’s default or programmed local clock signal when it’s free running. The IC locks to an external clock injected to the SYNC pin (external clock frequency recommended to be 10% higher than the free running frequency). The delay from the rising edge of the external clock signal to the PHASE rising edge is half of the free running switching
period pulse 220ns, (0.5tSW+220ns). The maximum external clock frequency is recommended to be 1.6 of the free running frequency.

When the part enters PFM pulse skipping mode, the synchronization function is shut off and also no clock signal output in SYNC pin.

With the SYNC pins simply connected together, multiple ISL85403s can be synchronized. The slave ICs automatically have 180° phase shift with respective to the master IC.

**PGOOD**
The PGOOD pin is output of an open-drain transistor (refer to “Block Diagram” on page 5). An external resistor is required to be pulled up to VCC for proper PGOOD function. At start-up, PGOOD will be turned HIGH (internal PGOOD open-drain transistor is turned off) with 128 cycles delay after soft-start is finished (soft-start ramp reaches 1.02V) and FB voltage is within OV/UV window (90%REF < FB < 110%REF).

At normal operation, PGOOD will be pulled low with 1 cycle (minimum) and 6 cycles (maximum) delay if any of the OV (110%) or UV (90%) comparator is tripped. The PGOOD will be released HIGH with 128 cycles delay after FB recovers to be within OV/UV window (90%REF < FB < 110%REF). When EN is pulled low or VCC is below POR, PGOOD is pulled low with no delay.

In the case when the PGOOD pin is pulled up by external bias supply instead of VCC of itself, when the part is disabled, the internal PGOOD open-drain transistor is off, the external bias supply can charge PGOOD pin HIGH. This should be known as false PGOOD reporting. At start-up when VCC rise from 0, PGOOD will be pulled low when VCC reaches 1V. After EN is pulled low and VCC is falling, the PGOOD internal open-drain transistor will open with high impedance when VCC falls below 1V. The time between EN pulled low and PGOOD OPEN depends on the VCC falling time to 1V.

**Fault Protection**

**Overcurrent Protection**
The overcurrent function protects against any overload condition and output short at worst case, by monitoring the current flowing through the upper MOSFET.

There are 2 current limiting thresholds. The first one IOC1 is to limit the high-side MOSFET peak current cycle-by-cycle. The current limit threshold is set to default at 3.6A with ILIMIT pin connected to GND or VCC, or left open. The current limit threshold can also be programmed by a resistor RLIM at ILIMIT pin to ground. Use Equation 14 to calculate the resistor.

\[
R_{LIM} = \frac{300000}{I_{OC1}[A]} + 0.018 \quad \text{(EQ. 14)}
\]

Note that IOC1 is higher with lower RLIM. The usable resistor value range to program OC1 peak current threshold is 40kΩ to 330kΩ. RLIM value out of this range is not recommended.

The second current protection threshold IOC2 is 15% higher than IOC1 mentioned previously. Instantly after the high-side MOSFET current reaches IOC2, the PWM is shut off after 2-cycle delay and the IC enters hiccup mode. In hiccup mode, the PWM is disabled for dummy soft-start duration equaling to 5 regular soft-start periods. After this dummy soft-start cycle, the true soft-start cycle is attempted again. The IOC2 offers a robust and reliable protection against the worst case conditions.

The frequency foldback is implemented for the ISL85403. When overcurrent limiting, the switching frequency is reduced to be proportional to output voltage in order to keep the inductor current under limit threshold during overload condition. The low limit of frequency under frequency foldback operation is 40kHz.

**Overvoltage Protection**
If the voltage detected on the FB pin is over 110% or 120% of reference, the high-side and low-side driver shuts down immediately and stays off until FB voltage drops to 0.8V. When the FB voltage drops to 0.8V, the drivers are released ON. 110% OVP is off during soft-start and active after soft-start is done. 120% OVP is active during and after soft-start.

**Thermal Protection**
The ISL85403 PWM will be disabled if the junction temperature reaches +160°C. There is +20°C hysteresis for OTP. The part will restart after the junction temperature drops below +140°C.

**Component Selections**
The ISL85403 iSim model can be used to simulate for both the time domain behaviors and small signal loop stability analysis.

**Output Capacitors - Buck**
An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are two critical factors when considering output capacitance choice. The current mode control loop allows for the usage of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors may also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the
manufacturers datasheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, they are a very good choice in many applications due to their reliability and extremely low ESR.

In buck topology, the following equations allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

\[ V_{\text{OUT,ripple}} = \frac{\Delta I}{8*f_{SW}*C_{\text{OUT}}} \]  
(EQ. 15)

where \(\Delta I\) is the inductor’s peak to peak ripple current, \(f_{SW}\) is the switching frequency and \(C_{\text{OUT}}\) is the output capacitor.

If using electrolytic capacitors then:

\[ V_{\text{OUT,ripple}} = \frac{\Delta I*ESR}{I_{\text{OUT}}} \]  
(EQ. 16)

Regarding transient response needs, a good starting point is to determine the allowable overshoot in \(V_{\text{OUT}}\) if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to \(C_{\text{OUT}}\) causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. The Equation 17 determines the required output capacitor value in order to achieve a desired overshoot relative to the regulated voltage.

\[ C_{\text{OUT}} = \frac{I_{\text{OUT}}^2*L}{(V_{\text{OUT}}^2MAX/V_{\text{OUT}}^2 - 1)} \]  
(EQ. 17)

where \(V_{\text{OUT}}_\text{MAX}/V_{\text{OUT}}\) is the relative maximum overshoot allowed during the removal of the load.

**Input Capacitors - Buck**

Depending on the system input power rail conditions, the aluminum electrolytic type capacitor is normally needed to provide the stable input voltage. Thus, restrict the switching frequency pulse current in a small area over the input traces for better EMC performance. The input capacitor should be able to handle the RMS current from the switching power devices.

Ceramic capacitors must be used at VIN pin of the IC and multiple capacitors including 1µF and 0.1µF are recommended. Place these capacitors as closely as possible to the IC.

**Output Inductor - Buck**

The inductor value determines the converter’s ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, \(\Delta I\). A reasonable starting point is 30% to 40% of total load current. The inductor value is calculated using Equation 18:

\[ L = \frac{V_{\text{IN}} - V_{\text{OUT}}}{f_{SW} \times \Delta I} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \]  
(EQ. 18)

Increasing the value of inductance reduces the ripple current and thus ripple voltage. However, the larger inductance value may reduce the converter’s response time to a load transient. The inductor current rating should be as such that it will not saturate in overcurrent conditions.

**Low-side Power MOSFET**

In synchronous buck application, a power N MOSFET is needed as the synchronous low-side MOSFET and a good one should have low Qgd, low \(r_{DS(ON)}\) and small \(R_g\) (\(R_g_{\text{typ}} < 1.5\Omega\) recommended). The Vgth_min is recommended to be or higher than 1.2V. A good example is SQS462EN.

A 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise.

**Output Voltage Feedback Resistor Divider**

The output voltage can be programmed down to 0.8V by a resistor divider from \(V_{\text{OUT}}\) to FB according to Equation 19.

\[ V_{\text{OUT}} = 0.8 \times \left( 1 + \frac{R_{\text{UP}}}{R_{\text{LOW}}} \right) \]  
(EQ. 19)

In an application requiring least input quiescent current, large resistors should be used for the divider. Generally, a resistor value of 10k to 300k can be used for the upper resistor.

**Boost Inductor (2-Stage Boost Buck)**

Besides the need to sustain the current ripple to be within a certain range (30% to 50%), the boost inductor current at its soft-start is a more important perspective to be considered in selection of the boost inductor. Each time the boost starts up, there is a fixed 500µs soft-start time when the duty cycle increases linearly from \(V_{\text{MIN(ON)}}*f_{SW}\) to ~50%. Before and after boost start-up, the boost output voltage will jump from \(V_{\text{IN,BOOST}}\) to voltage \((V_{\text{IN,BOOST}} + V_{\text{OUT,BUCK}})\). The design target in boost soft-start is to ensure the boost input current is sustained to minimum but capable to charge the boost output voltage to have a voltage step equaling to \(V_{\text{OUT,BUCK}}\). A big inductor will block the inductor current to increase and not high enough to be able to charge the output capacitor to the final steady state value \((V_{\text{IN,BOOST}} + V_{\text{OUT,BUCK}})\) within 500µs. A 6.8µH inductor is a good starting point for its selection in design. The boost inductor current at start-up must be checked by oscilloscope to ensure it is under an acceptable range. It is suggested to run the iSim model (use the ISL85403 iSim model available on the internet) to assist in the proper inductor value.

**Boost Output Capacitor (2-Stage Boost Buck)**

Based on the same theory in boost start-up previously described in the boost inductor selection, a large capacitor at boost output will cause high inrush current at boost PWM start-up. 22µF is a good choice for applications with a buck output voltage less than 10V. Also some minimum amount of capacitance has to be used in boost output to keep the system stable. It is suggested to run the iSim model, which is available on the internet to assist in designing the proper capacitor value.
Loop Compensation Design - Buck

The ISL85403 uses constant frequency peak current mode control architecture to achieve fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant and the system becomes single order system. It is much easier to design the compensator to stabilize the loop compared with voltage mode control. Peak current mode control has inherent input voltage feed-forward function to achieve good line regulation. Figure 28 shows the small signal model of a buck regulator.

PWM Comparator Gain $F_m$

The PWM comparator gain $F_m$ for peak current mode control is given by Equation 20:

$$F_m = \frac{d}{d_t} = \frac{1}{(S_e + S_n/T_s)}$$

(EQ. 20)

Where, $S_e$ is the slew rate of the slope compensation and $S_n$ is given by Equation 21:

$$S_n = R_t \frac{V_{in} - V_o}{L_p}$$

(EQ. 21)

where, $R_t$ is the gain of the current amplifier.

Current Sampling Transfer Function $He(S)$

In current loop, the current signal is sampled every switching cycle. It has the following transfer function in Equation 22:

$$He(S) = \frac{S^2}{\omega_n^2 + \frac{S}{\omega_n Q_n} + 1}$$

(EQ. 22)

where, $Q_n$ and $\omega_n$ are given by $Q_n = \frac{2}{\pi} \omega_n = \pi f_{SW}$

Power Stage Transfer Functions

Transfer function $F_1(S)$ from control to output voltage is:

$$F_1(S) = \frac{V_o}{V_{in}} = \frac{1 + \frac{S}{\omega_{esr}}}{\omega_o^2 + \frac{S}{\omega_o Q_p} + 1}$$

(EQ. 23)

where, $\omega_{esr} = \frac{1}{R_o C_o Q_p} = \frac{1}{\frac{C_o}{L_p} \omega_0}$.

Transfer function $F_2(S)$ from control to inductor current is given by Equation 24:

$$F_2(S) = \frac{i_L}{V_{in}} = \frac{V_{in}}{R_o + R_{LP} + 1 + \frac{S}{\omega_2}}$$

(EQ. 24)

where $\omega_2 = \frac{1}{R_o C_o}$.

Current loop gain $T_i(S)$ is expressed as Equation 25:

$$T_i(S) = R_t F_m F_2(S) H_e(S)$$

(EQ. 25)

The voltage loop gain with open current loop is expressed in Equation 26:

$$T_v(S) = K F_m F_1(S) A_v(S)$$

(EQ. 26)

The Voltage loop gain with current loop closed is given by Equation 27:

$$L_v(S) = \frac{T_v(S)}{1 + T_i(S)}$$

(EQ. 27)

If $T_i(S) >> 1$, then Equation 27 can be simplified as Equation 28:

$$L_v(S) = \frac{R_o + R_{LP} + 1 + \frac{S}{\omega_{esr} A_v(S)}}{1 + \frac{S}{\omega_p}}$$

(EQ. 28)

Equation 28 shows that the system is a single order system. Therefore, a simple type II compensator can be easily used to stabilize the system. A type III compensator is needed to expand the bandwidth for current mode control in some cases.

FIGURE 29. TYPE III COMPENSATOR
A compensator with 2 zeros and 1 pole is recommended for this part, as shown in Figure 29. Its transfer function is expressed as Equation 29:

\[
A_c(S) = \frac{V_{comp}}{V_O} = \frac{1}{SR_1C_1} \left( \frac{1 + \frac{S}{\omega_{cz1}}}{1 + \frac{S}{\omega_{cz2}}} \right) \left( \frac{1 + \frac{S}{\omega_{cp}}}{1 + \frac{S}{\omega_{cp}}} \right) \quad (\text{EQ. 29})
\]

where,

\[
\omega_{cz1} = \frac{1}{R_2C_1}, \quad \omega_{cz2} = \frac{1}{(R_1 + R_3)C_3}, \quad \frac{1}{\omega_{cp}} = \frac{1}{R_3C_3}
\]

Compensator design goal:
Loop bandwidth \(f_c\): \(\frac{1}{4f_{SW}}\)
Gain margin: >10dB
Phase margin: 45°

The compensator design procedure is as follows:

1. Position \(\omega_{cz2}\) and \(\omega_{cp}\) to derive \(R_3\) and \(C_3\).

   Put the compensator zero \(\omega_{cz2}\) at \((1 \text{ to } 3)/(RoCo)\)

   Put the compensator pole \(\omega_{cp}\) at ESR zero or \(0.35\text{ to } 0.5\) times of switching frequency, whichever is lower. In all-ceramic-cap design, the ESR zero is normally higher than half of the switching frequency. \(R_3\) and \(C_3\) can be derived as follows:

   **Case A:** ESR zero \(\frac{1}{2\pi R_c C_o}\) less than \((0.35 \text{ to } 0.5)f_{SW}\)

   \[
   C_3 = \frac{R_o C_o - 3R_c C_o}{3R_1} \quad (\text{EQ. 31})
   \]

   \[
   R_3 = \frac{3R_c R_1}{R_o - 3R_c} \quad (\text{EQ. 32})
   \]

   **Case B:** ESR zero \(\frac{1}{2\pi R_c C_o}\) larger than \((0.35 \text{ to } 0.5)f_{SW}\)

   \[
   C_3 = \frac{0.33R_o C_o f_{SW} - 0.46}{f_{SW} R_1} \quad (\text{EQ. 33})
   \]

   \[
   R_3 = \frac{0.73R_o C_o f_{SW}}{1} \quad (\text{EQ. 34})
   \]

2. Derive \(R_2\) and \(C_1\).

   The loop gain \(L_v(S)\) at cross over frequency of \(f_c\) has unity gain. Therefore, \(C_1\) is determined by Equation 35.

   \[
   C_1 = \frac{(R_1 + R_3)C_3}{2\pi f_c R_1 R_3 C_o} \quad (\text{EQ. 35})
   \]

   The compensator zero \(\omega_{cz1}\) can boost the phase margin and bandwidth. To put \(\omega_{cz1}\) at 2 times of cross over frequency \(f_c\) is a good start point. It can be adjusted according to specific design. \(R_4\) can be derived from Equation 36.

   \[
   R_2 = \frac{1}{4\pi f_c C_1} \quad (\text{EQ. 36})
   \]

Example: \(V_{IN} = 12V, V_o = 5V, I_o = 2A, f_{SW} = 500kHz, C_o = 60\mu F/3m\Omega, L = 10\mu H, R_1 = 0.20V/A, f_c = 50kHz, R_1 = 105k, R_{BIAS} = 20k\Omega\).

Select the crossover frequency to be 35kHz. Since the output capacitors are all ceramic, use **Equations 33** and **34** to derive \(R_3\) to be 20k and \(C_3\) to be 470pF.

Then use **Equations 35** and **36** to calculate \(C_1\) to be 180pF and \(R_2\) to be 12.7k. Select 150pF for \(C_1\) and 15k for \(R_2\).

There is approximately 30pF parasitic capacitance between COMP to FB pins that contributes to a high frequency pole. Any extra external capacitor is not recommended between COMP and FB.

**Figure 30** shows the simulated bode plot of the loop. It is shown that it has 26kHz loop bandwidth with 70° phase margin and -28 dB gain margin.

Note in applications where the PFM mode is desired especially when type III compensation network is used, the value of the capacitor between the COMP pin and the FB pin (not the capacitor in series with the resistor between COMP and FB) should be minimal to reduce the noise coupling for proper PFM operation. No external capacitor between COMP and FB is recommended at PFM applications.

In PFM mode operations, a RC filter from FB to ground (R in series with C, connecting from FB to ground) may help to reduce the noise effects injected to FB pin. The recommended values for the filter is 499\(\Omega\) to 1k for the R and 470pF for the C.
Loop Compensation Design for 2-Stage Boost Buck and Single-stage Buck Boost

For 2-stage boost buck and single-stage non-inverting buck boost configurations, it's highly recommended to use the iSim model (use the ISL85403 iSim model available in internet) to evaluate the loop bandwidth and phase margin.

Layout Suggestions

1. Place the input ceramic capacitors as closely as possible to the IC VIN pin and power ground connecting to the power MOSFET or Diode. Keep this loop (input ceramic capacitor, IC VIN pin and MOSFET/Diode) as tiny as possible to achieve the least voltage spikes induced by the trace parasitic inductance.

2. Place the input aluminum capacitors closely as possible to the IC VIN pin.

3. Keep the phase node copper area small but large enough to handle the load current.

4. Place the output ceramic and aluminum capacitors close to the power stage components as well.

5. Place vias (≥9) in the bottom pad of the IC. The bottom pad should be placed in ground copper plane with an area as large as possible in multiple layers to effectively reduce the thermal impedance.

6. Place the 4.7µF ceramic decoupling capacitor at the VCC pin (the closest place to the IC). Put multiple vias (≥3) close to the ground pad of this capacitor.

7. Keep the bootstrap capacitor close to the IC.

8. Keep the LGATE drive trace as short as possible and try to avoid using via in the LGATE drive path to achieve the lowest impedance.

9. Place the positive voltage sense trace close to the place to be strictly regulated.

10. Place all the peripheral control components close to the IC.

---

FIGURE 30. SIMULATED LOOP BODE PLOT

FIGURE 31. PCB VIA PATTERN
## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>CHANGE</th>
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<tbody>
<tr>
<td>March 13, 2015</td>
<td>FN8631.1</td>
<td>Changed the max input Voltage (Vin) from 36V to 40V on the following pages:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On page 1: In the description and features sections</td>
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<tr>
<td></td>
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<td>On page 4: VIN pin description</td>
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<td></td>
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<td>On page 7: Recommended operating conditions for VIN</td>
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<tr>
<td></td>
<td></td>
<td>On page 15: Application description for the “Input Voltage” section</td>
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<tr>
<td></td>
<td></td>
<td>On page 1, added “Related Literature” section.</td>
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<tr>
<td></td>
<td></td>
<td>On page 4, added ISL85403EVAL2Z to the Ordering Information table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Replaced Figures 5 and 6.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Removed Figures 10 and 11 and the references on page 15.</td>
</tr>
<tr>
<td>March 12, 2014</td>
<td>FN8631.0</td>
<td>Initial Release</td>
</tr>
</tbody>
</table>

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## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company’s products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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Reliability reports are also available from our website at [www.intersil.com/support](http://www.intersil.com/support).
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.