EL1503

High Power Differential Line Driver

FN7038
Rev 0.00
July 17, 2001

The EL1503 ADSL Line Driver contains two wideband high-voltage drivers which are ideally suited for both ADSL and HDSL2 applications. They can supply a 39.2V_{P-P} signal into a 22Ω load while exhibiting very low distortion. The EL1503 also has a number of power saving features. The I_{ADJ} pin can be used to set the maximum supply current and the C_0 and C_1 pins can be used to digitally vary the supply current to one of four modes. These modes include full power, low power, terminate only and power down.

The EL1503 uses current-feedback type amplifiers, which achieve a high slew rate while consuming moderate power. They retain their frequency response over a wide range of externally set gains. The EL1503 operates on ±5V to ±12V supplies and consumes only 12.5mA per amplifier.

The device is supplied in a standard form-factor 20-pin SO (0.300”), 16-pin thermal SO (0.150”), and the small footprint (4x5mm) 24-pin LPP packages. Center pins on each side of the 20-pin and 16-pin packages are used as ground connections and heat spreaders. The LPP package has the potential for a low θ_{JA} (<40°C/W) and dissipates heat by means of a thermal pad that is soldered onto the PCB. All package options are specified for operation over the full -40°C to +85°C temperature range.

Features

- High power ADSL driver
- 39.2V_{P-P} differential output drive into 22Ω
- 42.4V_{P-P} differential output drive into 65Ω
- Driver 2nd/3rd harmonics of -66dBc/-72dBc at 2V_{P-P} into 100Ω differential
- Supply current of 12.5mA per amplifier
- Supply current control
- Power saving modes
- Standard surface-mount packages
- Ultra-small LPP package

Applications

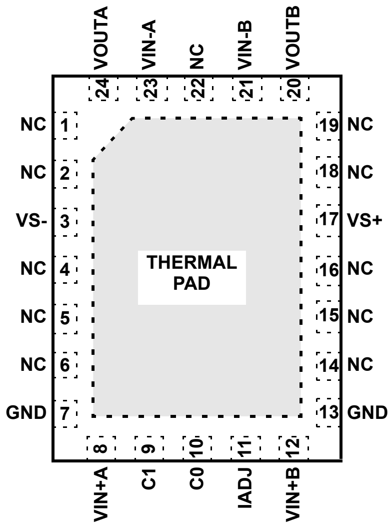
- ADSL line drivers
- HDSL2 line drivers
- Video distribution amplifiers

Ordering Information

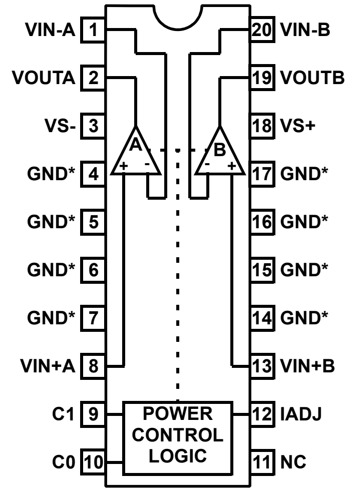
PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL1503CL	24-Pin LPP	-	MDP0046
EL1503CL-T7	24-Pin LPP	7”	MDP0046
EL1503CL-T13	24-Pin LPP	13”	MDP0046
EL1503CM	20-Pin SO (0.300")	-	MDP0027
EL1503CM-T13	20-Pin SO (0.300")	13”	MDP0027
EL1503CS	16-Pin SO (0.150”)	-	MDP0027
EL1503CS-T7	16-Pin SO (0.150”)	7”	MDP0027
EL1503CS-T13	16-Pin SO (0.150”)	13”	MDP0027

Pinouts

EL1503
(24-PIN LPP)
TOP VIEW

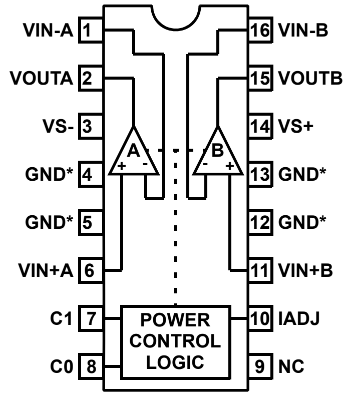


EL1503
[20-PIN SO (0.300")]
TOP VIEW



*GND pins are heat spreaders

EL1503
[16-PIN SO (0.150")]
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

V_S+ to V_{S}- Supply Voltage 26.4V
V_S+ Voltage to Ground . . . . . -0.3V to +26.4V
V_S- Voltage to Ground . . . . . -26.4V to 0.3V
Input C_0/C_1 to Ground 7V
Driver V_{IN}+ Voltage . . . . . V_S- to V_S+
Current into Any Input 8mA
Output Current from Driver (Static) 100mA
Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -60°C to +150°C
Operating Junction Temperature . . . . . -40°C to +150°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = ±12V, R_F = 1.5kΩ, R_L = 65Ω, I_{ADJ} = C_0 = C_1 = 0V, T_A = 25°C. Amplifiers tested separately.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_S+(Full Power)	Positive Supply Current per Amplifier	All Outputs at 0V, C_0 = C_1 = 0V	10	12.5	16	mA
I_S-(Full Power)	Negative Supply Current per Amplifier	All Outputs at 0V, C_0 = C_1 = 0V	-15	-11.5	-9	mA
I_S+(Low Power)	Positive Supply Current per Amplifier	All Outputs at 0V, C_0 = 5V, C_1 = 0V	7	9	11.5	mA
I_S-(Low Power)	Negative Supply Current per Amplifier	All Outputs at 0V, C_0 =5V, C_1 = 0V	-10.5	-8	-6	mA
I_S+(Terminate)	Positive Supply Current per Amplifier	All Outputs at 0V, C_0 = 0V, C_1 = 5V	4	5.1	7	mA
I_S-(Terminate)	Negative Supply Current per Amplifier	All Outputs at 0V, C_0 = 0V, C_1 = 5V	-6	-4	-3	mA
I_S+(Power Down)	Positive Supply Current per Amplifier	All Outputs at 0V, C_0 = C_1 = 5V	0.75	1.05	1.7	mA
I_S-(Power Down)	Negative Supply Current per Amplifier	All Outputs at 0V, C_0 = C_1 = 5V	-0.5	-0.25	0.07	mA
I_{GND}	Gnd Supply Current per Amplifier	All Outputs at 0V		-1		mA
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage		-30		30	mV
ΔV_{OS}	V_{OS} Mismatch		-15		15	mV
I_B+	Non-Inverting Input Bias Current		-15		15	µA
I_B-	Inverting Input Bias Current		-50		50	µA
ΔI_B-	I_B- Mismatch		-30		30	µA
R_{OL}	Transimpedance		0.4	0.8		MΩ
e_N	Input Noise Voltage			4.5		nV/√Hz
i_N	-Input Noise Current			13		pA/√Hz
V_{IH}	Input High Voltage	C_0 & C_1 inputs	2.7			V
V_{IL}	Input Low Voltage	C_0 & C_1 inputs			0.8	V
I_{IH1}	Input High Current for C_1	C_1 = 5V	1.5		8	µA
I_{IH0}	Input High Current for C_0	C_0 = 5V	0.75		4	µA
I_{IL}	Input Low Current for C_1 or C_0	C_1 = 0V, C_0 = 0V	-1		1	µA

Electrical Specifications V_S = ±12V, R_F = 1.5kΩ, R_L= 65Ω, I_{ADJ} = C_0 = C_1 = 0V, T_A = 25°C. Amplifiers tested separately. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing	R_L = 65Ω	±10.3	±10.6		V
		R_L = 22Ω	±9.3	±9.8		V
I_{OL}	Linear Output Current	A_V = 5, R_L=10Ω, f=100kHz, THD=-60dBc		450		mA
I_{OUT}	Output Current	V_{OUT} = IV, R_L = 1Ω		1		A
DYNAMIC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +5		80		MHz
HD2	2nd Harmonic Distortion	f_C = 1MHz, R_L = 100Ω, V_{OUT} = 2V_{P-P}		-66		dBc
		f_C = 1MHz, R_L = 25Ω, V_{OUT} = 2V_{P-P}		-61		dBc
HD3	3rd Harmonic Distortion	f_C = 1MHz, R_L = 100Ω, V_{OUT} = 2V_{P-P}		-77		dBc
		f_C = 1MHz, R_L = 25Ω, V_{OUT} = 2V_{P-P}		-72		dBc
SR	Slewrate	V_{OUT} from -8V to +8V Measured at ±4V	700	1100		V/µS

Typical Performance Curves

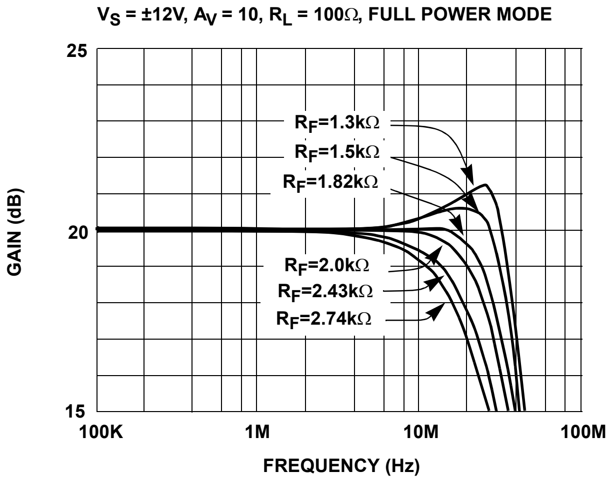


FIGURE 1. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

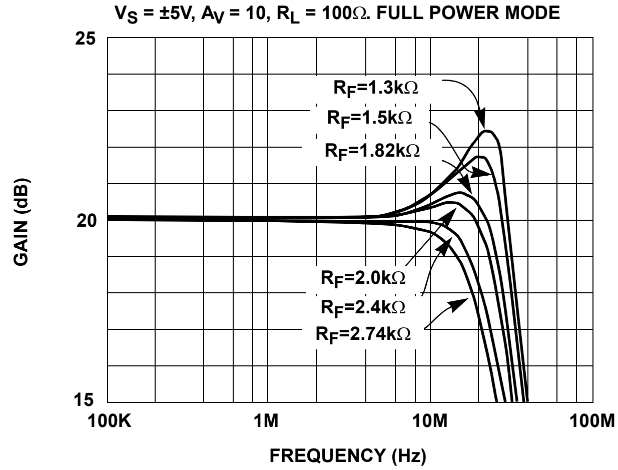


FIGURE 2. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

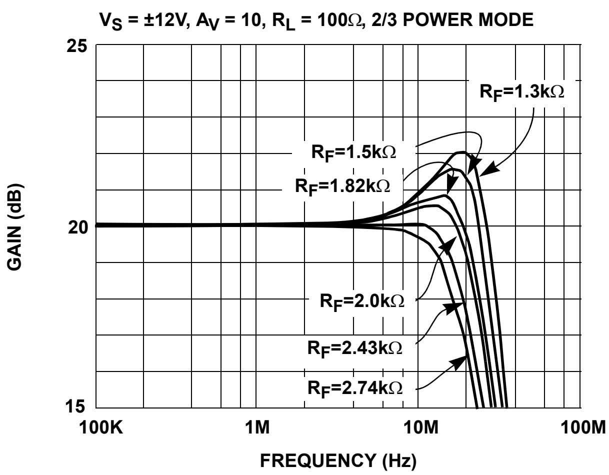


FIGURE 3. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

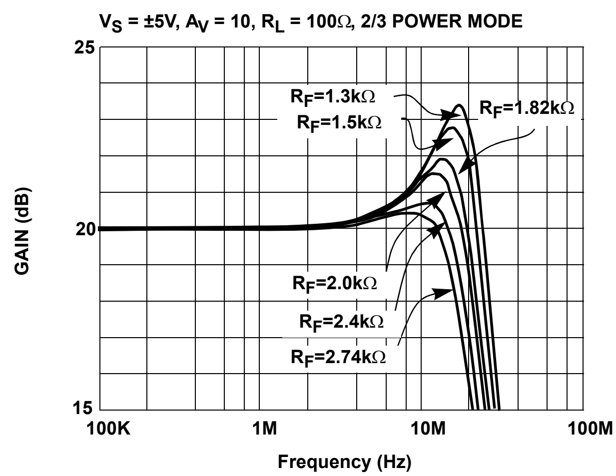


FIGURE 4. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

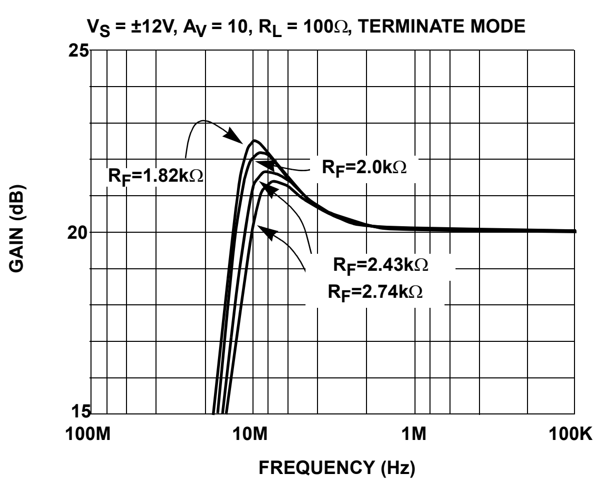


FIGURE 5. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

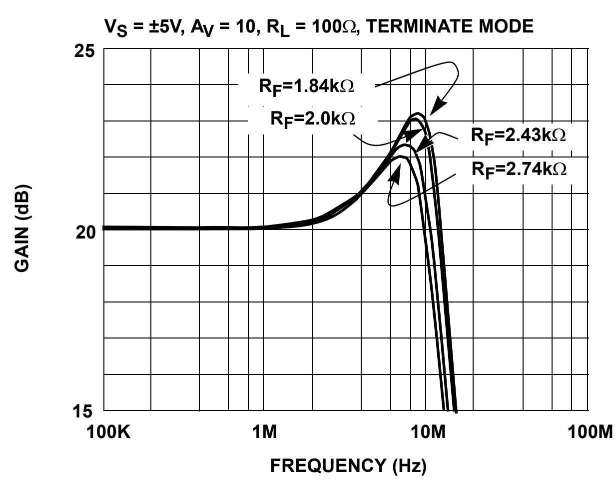


FIGURE 6. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

Typical Performance Curves (Continued)

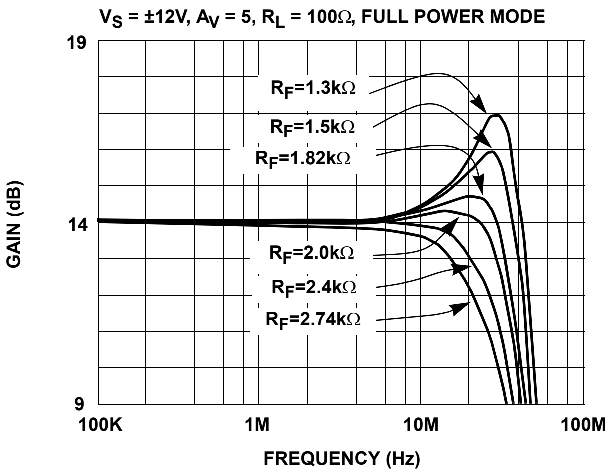


FIGURE 7. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

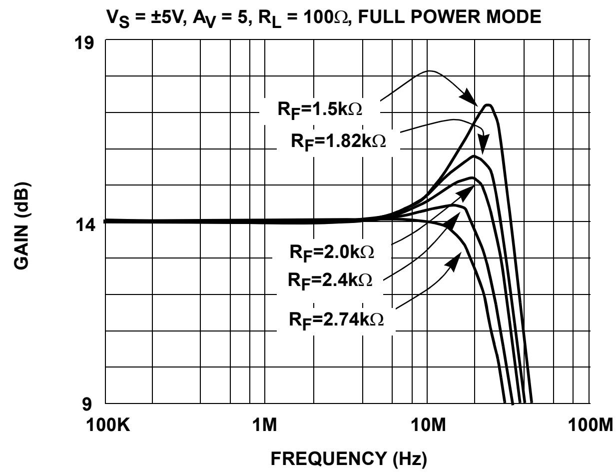


FIGURE 8. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

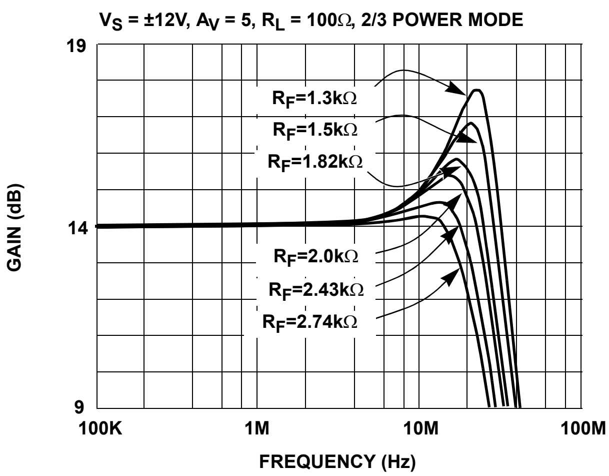


FIGURE 9. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

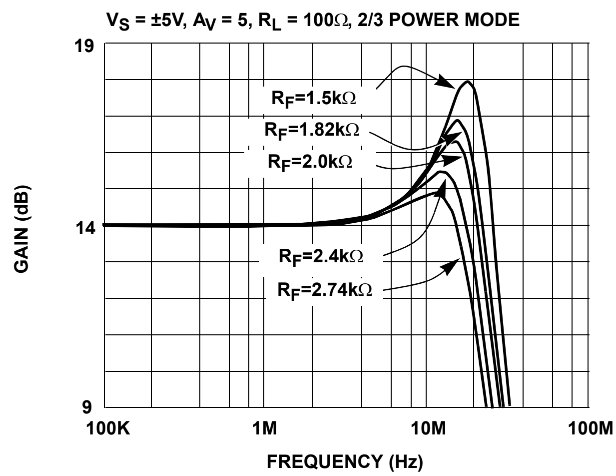


FIGURE 10. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

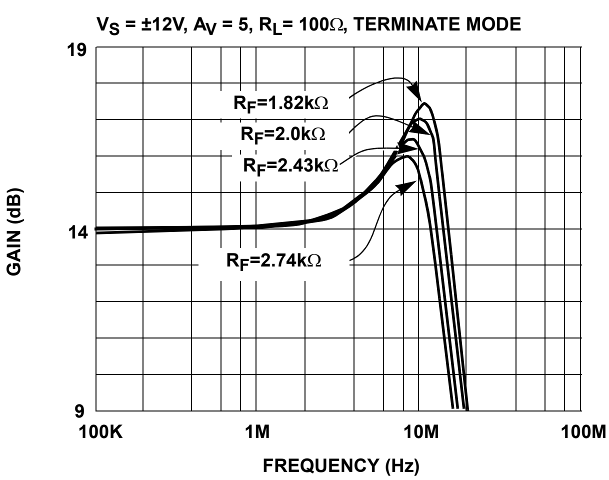


FIGURE 11. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

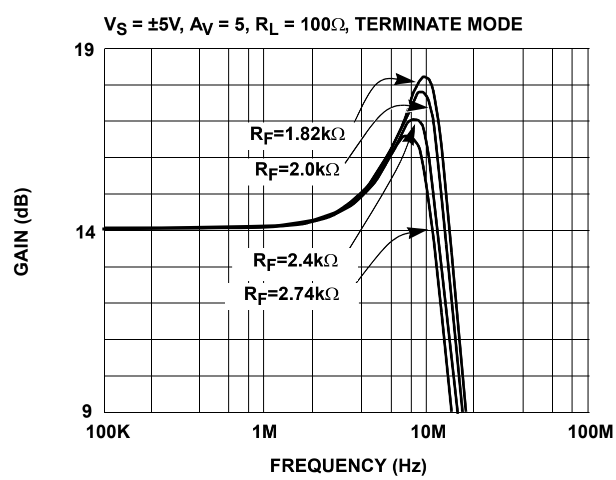


FIGURE 12. DRIVER DIFFERENTIAL FREQUENCY RESPONSE vs R_F

Typical Performance Curves (Continued)

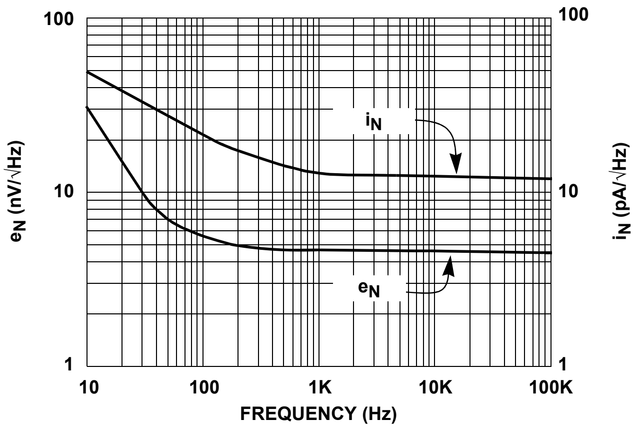


FIGURE 13. DRIVER INPUT VOLTAGE and FEEDBACK CURRENT NOISE vs FREQUENCY

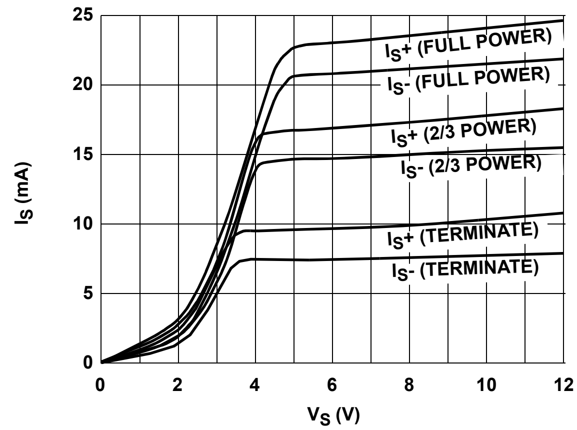


FIGURE 14. SUPPLY CURRENT vs SUPPLY VOLTAGE

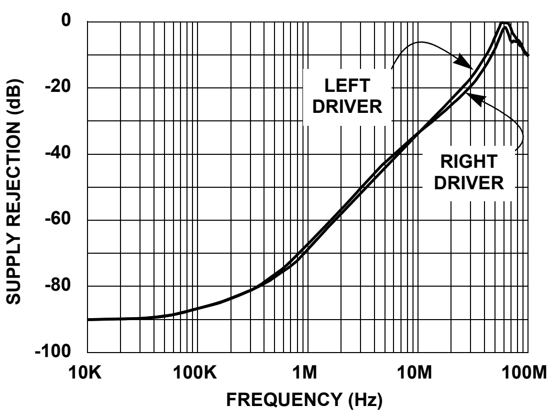


FIGURE 15. POSITIVE SUPPLY REJECTION vs FREQUENCY

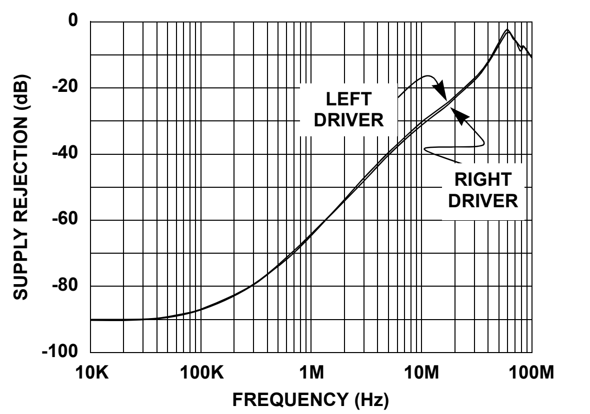


FIGURE 16. NEGATIVE SUPPLY REJECTION vs FREQUENCY

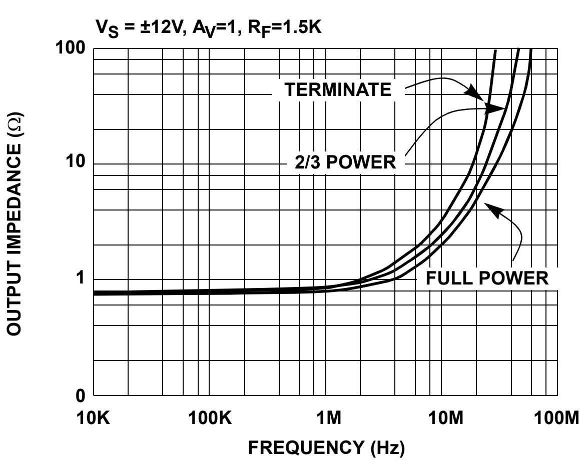


FIGURE 17. OUTPUT IMPEDANCE vs FREQUENCY

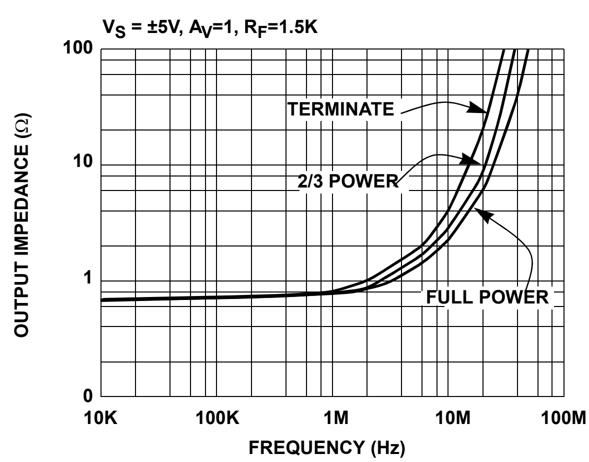


FIGURE 18. OUTPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

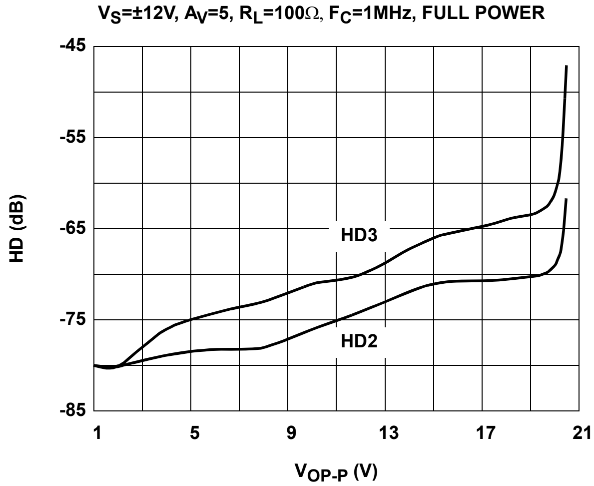


FIGURE 19. DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

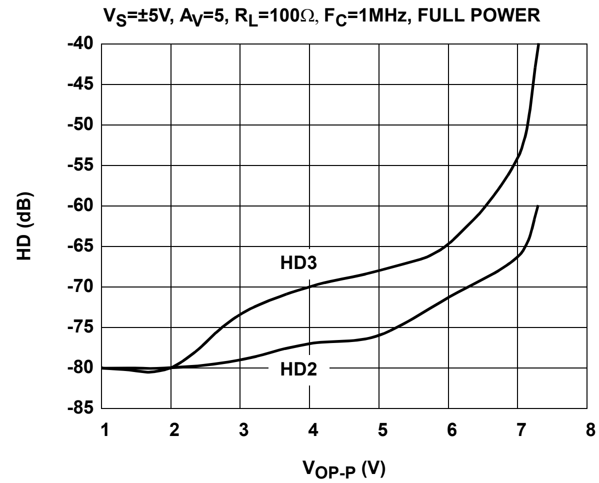


FIGURE 20. DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

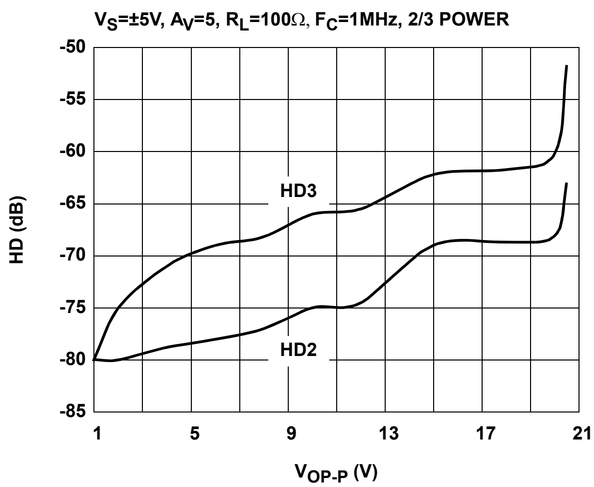


FIGURE 21. DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

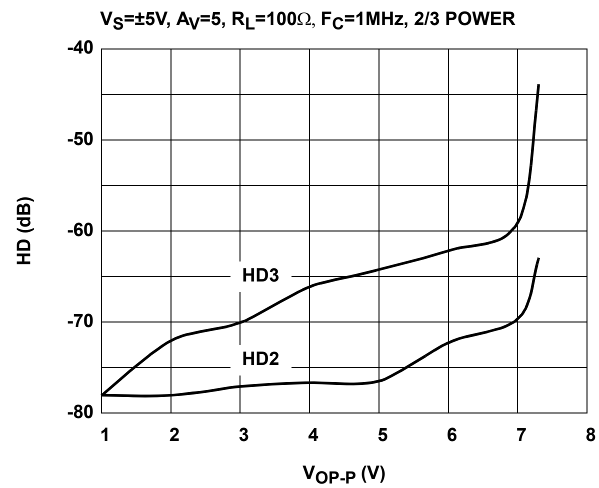


FIGURE 22. DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

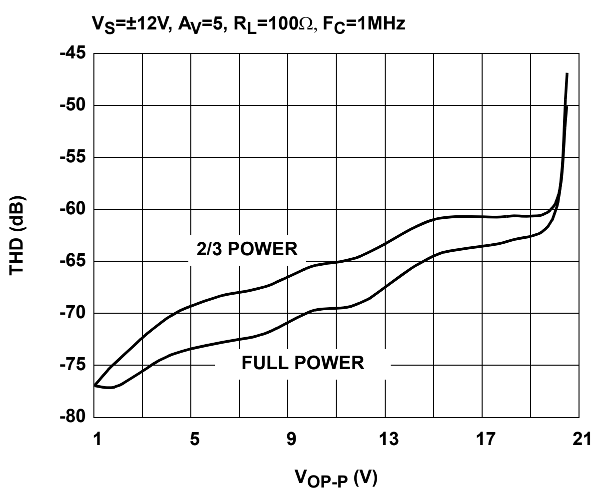


FIGURE 23. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

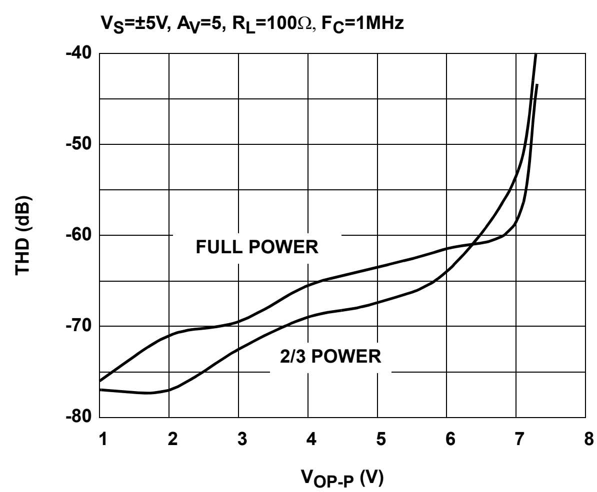


FIGURE 24. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

Typical Performance Curves (Continued)

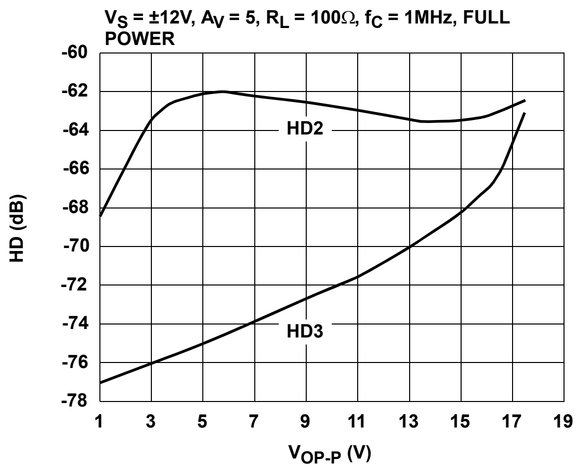


FIGURE 25. DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

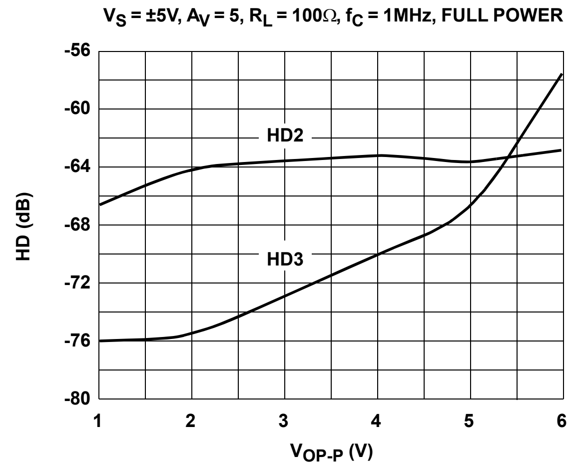


FIGURE 26. DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

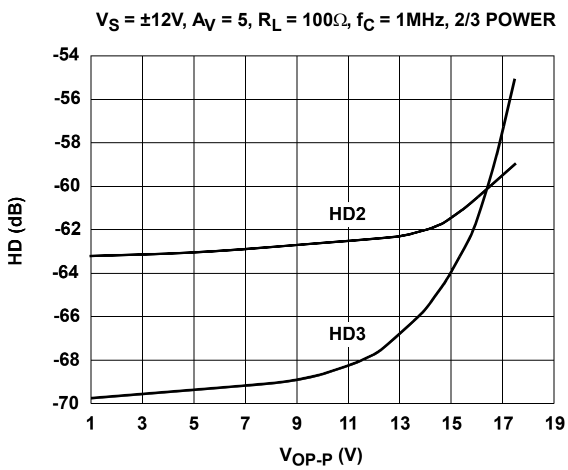


FIGURE 27. DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

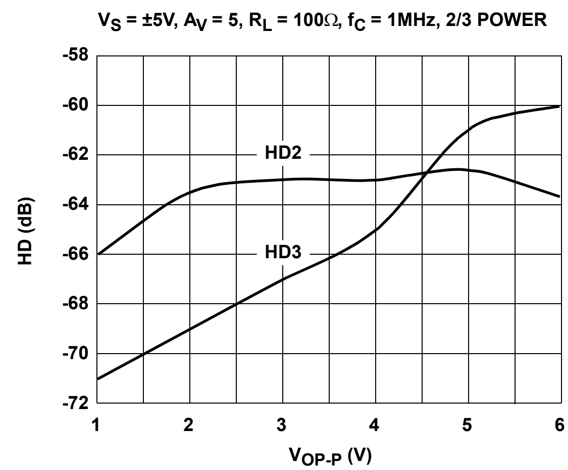


FIGURE 28. DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

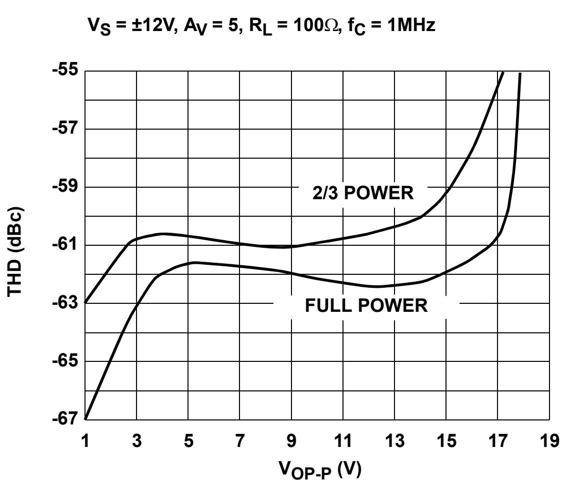


FIGURE 29. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

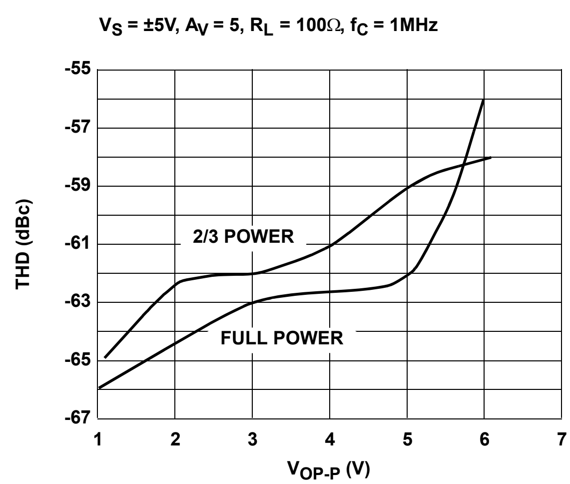


FIGURE 30. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs OUTPUT AMPLITUDE

Typical Performance Curves (Continued)

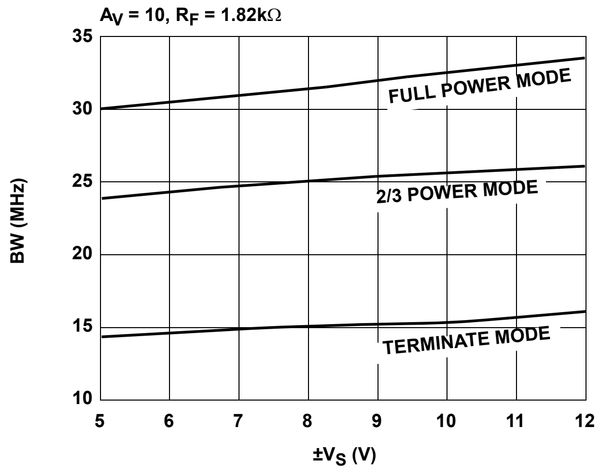


FIGURE 31. DIFFERENTIAL BANDWIDTH vs SUPPLY VOLTAGE

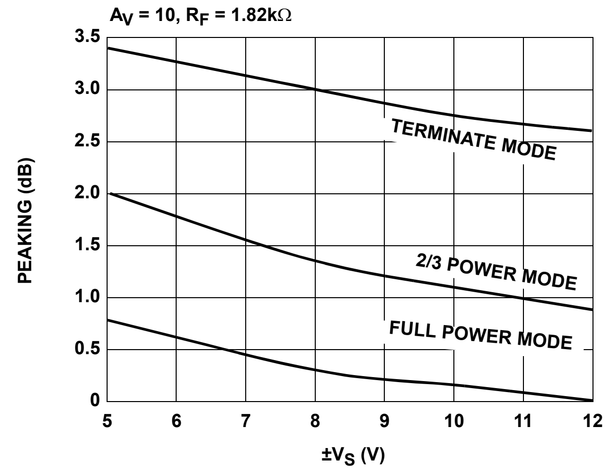


FIGURE 32. DIFFERENTIAL PEAKING vs SUPPLY VOLTAGE

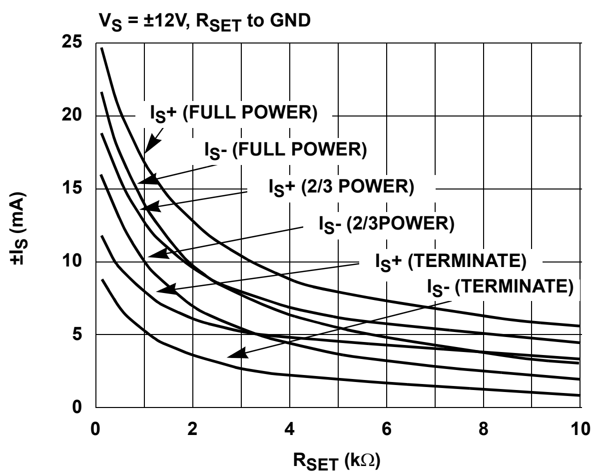


FIGURE 33. I_S vs R_{SET}

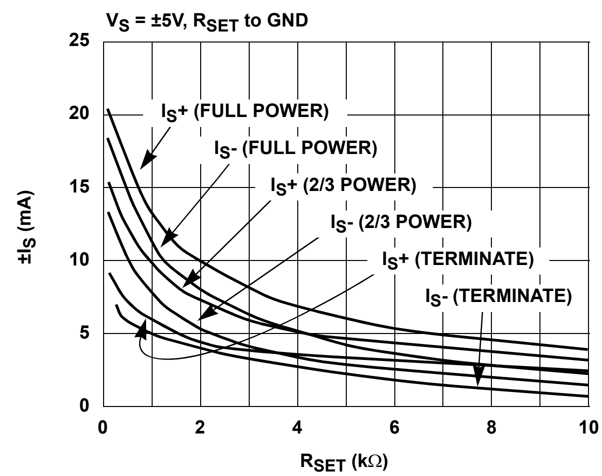


FIGURE 34. I_S vs R_{SET}

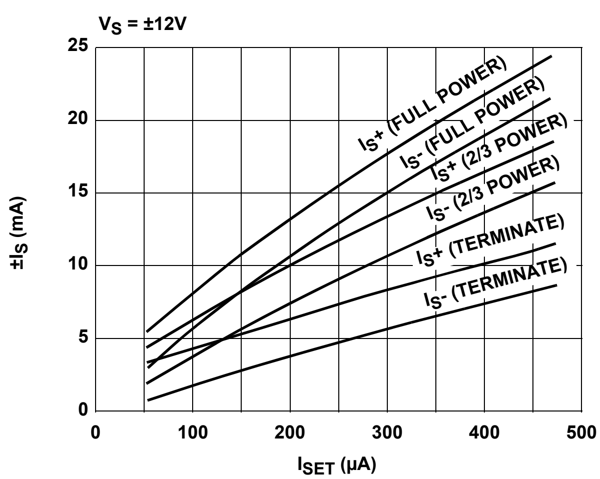


FIGURE 35. I_S vs I_{SET}

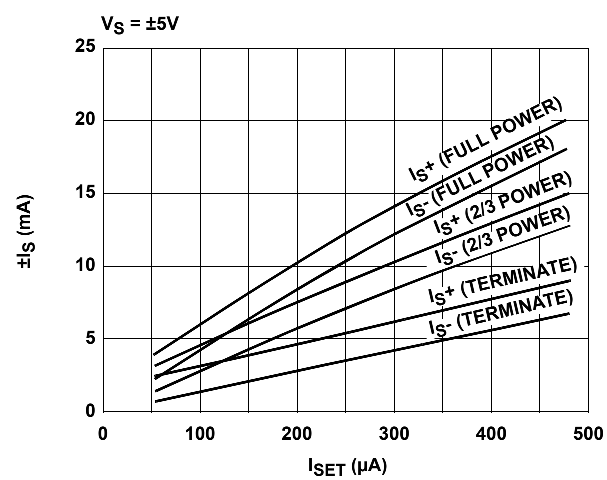


FIGURE 36. I_S vs I_{SET}

Typical Performance Curves (Continued)

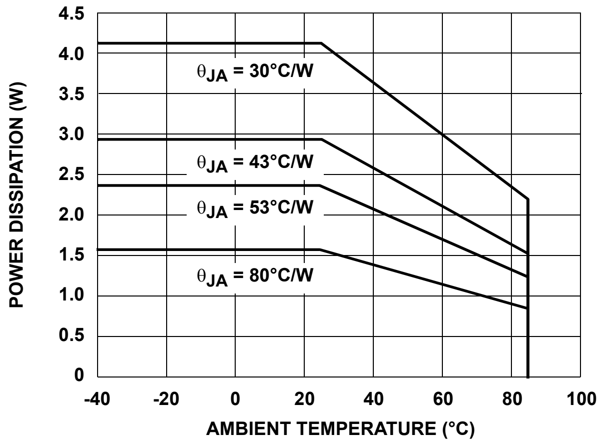


FIGURE 37. POWER DISSIPATION vs AMBIENT TEMPERATURE for VARIOUS MOUNTED θ_{JA}s

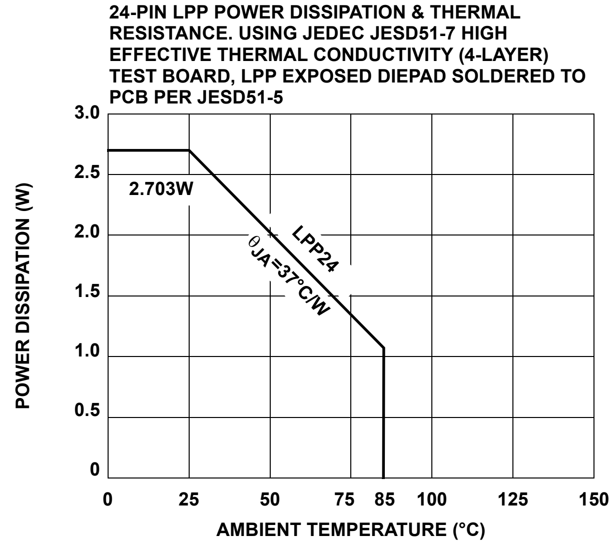


FIGURE 38. POWER DISSIPATION vs AMBIENT TEMPERATURE

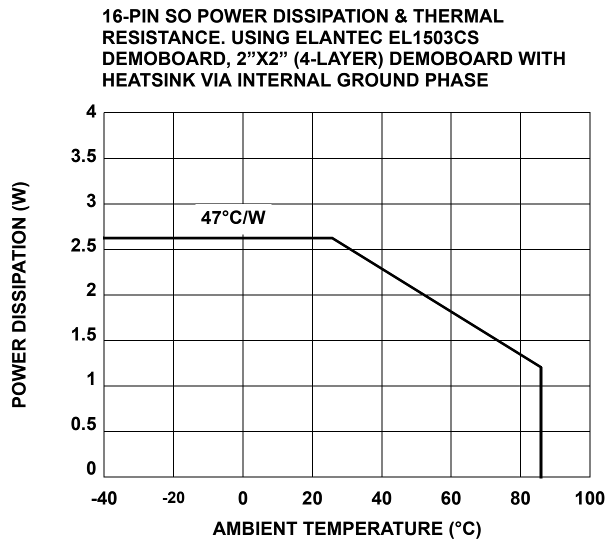
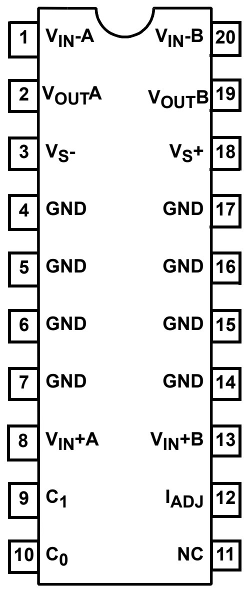
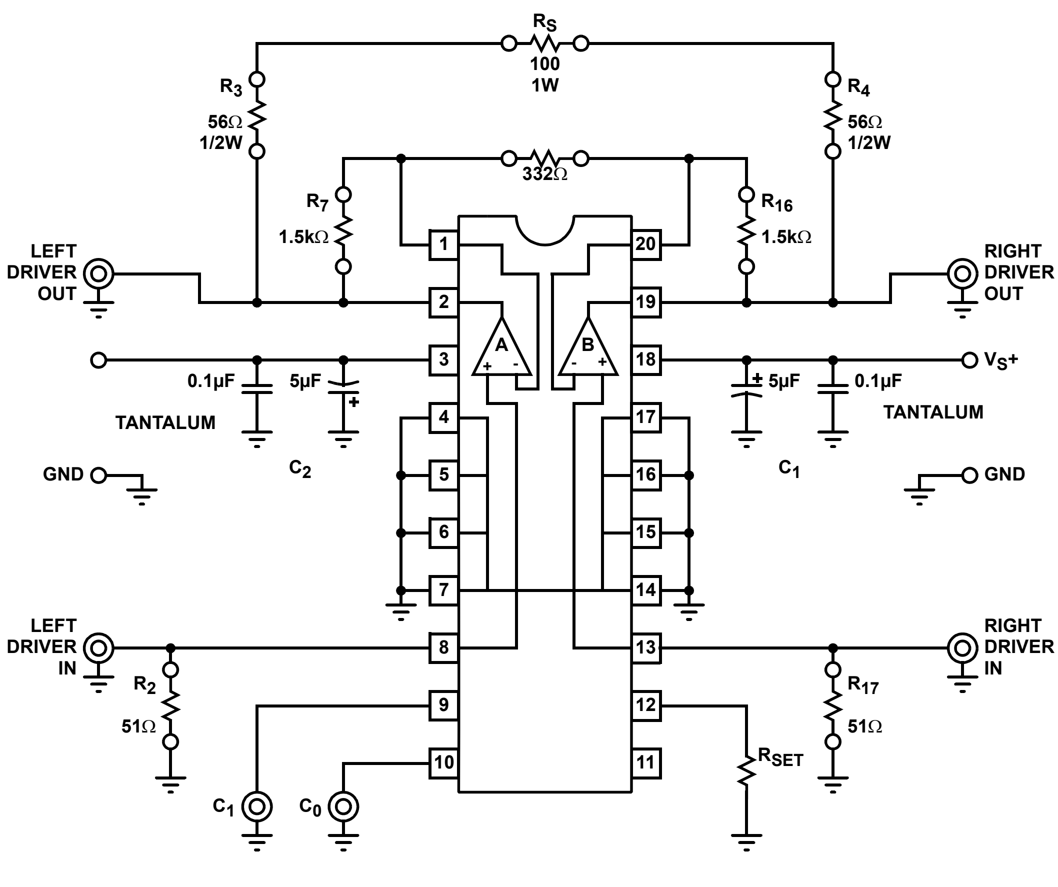


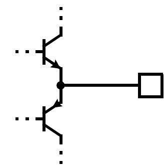
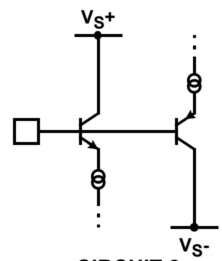
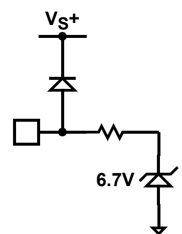
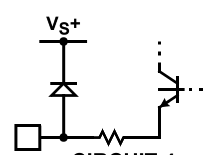
FIGURE 39. POWER DISSIPATION vs AMBIENT TEMPERATURE

Test Circuit





Pin Descriptions

16-PIN SO (0.150")	20-PIN SO (0.300")	24-PIN LPP	PIN NAME	FUNCTION	CIRCUIT
1	1	23	V_{IN}-A	Channel A Inverting Input	 CIRCUIT 1
2	2	24	V_{OUT}A	Channel A Output	(Reference Circuit 1)
3	3	3	V_S-	Negative Supply	
4, 5	4, 5, 6, 7	7	GND	Ground Connection	
6	8	8	V_{IN}+A	Channel A Non-Inverting Input	 CIRCUIT 2
7	9	9	C_1	Current Control Bit 1	 CIRCUIT 3
8	10	10	C_0	Current Control Bit 0	(Reference Circuit 3)
9	11	1, 2, 4, 5, 6, 14, 15, 16, 18, 19, 22	NC	Not Connected	
10	12	11	I_{ADJ}	Supply Current Control Pin	 CIRCUIT 4
11	13	12	V_{IN}+B	Channel B Non-Inverting Input	(Reference Circuit 2)
12, 13	14, 15, 16, 17	13	GND	Ground Connection	
14	18	17	V_S+	Positive Supply	
15	19	20	V_{OUT}B	Channel B Output	(Reference Circuit 1)
16	20	21	V_{IN}-B	Channel B Inverting Input	(Reference Circuit 1)

Applications Information

The EL1503 consists of two high-power line driver amplifiers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with signals up to 4MHz and produce low distortion levels. A typical interface circuit is shown in Figure 40 below.

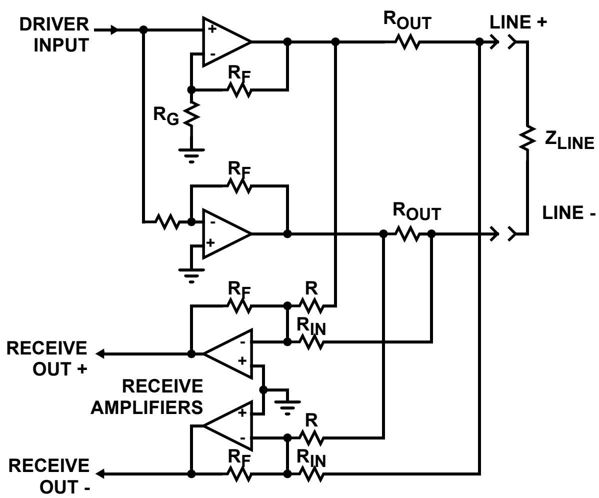


FIGURE 40. TYPICAL LINE INTERFACE CONNECTION

The amplifiers are wired with one in positive gain and the other in a negative gain configuration to generate a differential output for a single-ended input. They will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers R_F's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver. If a differential signal is available to the drive amplifiers, they may be wired so:

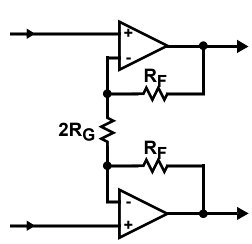


FIGURE 41. DRIVERS WIRED FOR DIFFERENTIAL INPUT

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The EL1503 amplifiers are somewhat sensitive to source impedance. In particular, they do not like being driven by inductive sources. More than 100nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4” of unshielded wiring, or 6” of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Power Supplies & Dissipation

Due to the high power drive capability of the EL1503, much attention needs to be paid to power dissipation. The power that needs to be dissipated in the EL1503 has two main contributors. The first is the quiescent current dissipation. The second is the dissipation of the output stage.

The quiescent power in the EL1503 is not constant with varying outputs. In reality, 7mA of the 12.5mA needed to power each driver is converted in to output current. Therefore, in the equation below we should subtract the average output current, I_O, or 7mA, whichever is the lowest. We'll call this term I_X.

Therefore, we can determine a quiescent current with the equation:

$$P_{Dquiescent} = V_S \times (I_S - 2I_X)$$

where:

V_S is the supply voltage (V_S+ to V_S-)

I_S is the maximum quiescent supply current (I_S+ + I_S-)

I_X is the lesser of I_O or 7mA (generally I_X = 7mA)

The dissipation in the output stage has two main contributors. Firstly, we have the average voltage drop across the output transistor and secondly, the average output current. For minimal power dissipation, the user should select the supply voltage and the line transformer ratio accordingly. The supply voltage should be kept as low as possible, while the transformer ratio should be selected so that the peak voltage required from the EL1503 is close to the maximum available output swing. There is a trade of however with the selection of transformer ratio. As the ratio is increased, the receive signal available to the receivers is reduced.

Once the user has selected the transformer ratio, the dissipation in the output stages can be selected with the following equation:

$$P_{Dtransistors} = 2 \times \overline{I_O} \times \left(\frac{V_S}{2} - \overline{V_O}\right)$$

where:

V_S is the supply voltage (V_S+ to V_S-)

V_O is the average output voltage per channel

I_O is the average output current per channel

The overall power dissipation (P_{DISS}) is obtained by adding $P_{Dquiescent}$ and $P_{Dtransistor}$.

Then, the θ_{JA} requirement needs to be calculated. This is done using the equation:

$$\theta_{JA} = \frac{(T_{JUNCT} - T_{AMB})}{P_{DISS}}$$

where:

T_{JUNCT} is the maximum die temperature (150°C)

T_{AMB} is the maximum ambient temperature

P_{DISS} is the dissipation calculated above

θ_{JA} is the junction to ambient thermal resistance for the package when mounted on the PCB

This θ_{JA} value is then used to calculate the area of copper needed on the board to dissipate the power. The graph below show various θ_{JA} for the SO20 mounted on different copper foil areas.

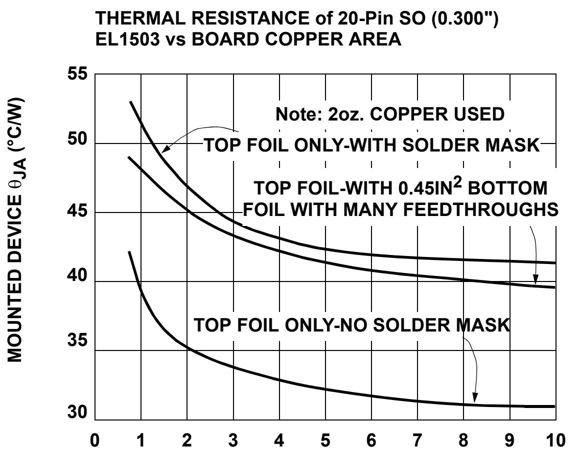


FIGURE 42. AREA OF CIRCUIT BOARD HEAT SINK (IN2)

A separate application note details the 24-pin LPP PCB design considerations.

Single Supply Operation

The EL1503 can also be powered from a single supply voltage. When operating in this mode, the GND pins can still be connected directly to GND. To calculate power dissipation, the equations in the previous section should be used, with V_S equal to half the supply rail.

EL1503 PCB Design

A separate application note details the 24-pin LPP PCB design considerations. The SO power packages (16 and 20 leads) are designed so that heat may be conducted away from the device in an efficient manner. To disperse this heat, the center leads (4 per side for the 20 lead and 2 per side for the 16 lead) are internally connected to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreads and convects to air. Thus, the ground plane on the component side of the board becomes the heatsink. This has proven to be a very effective technique, but several aspects of board layout should be noted. First, the heat should not be shunted to internal copper layers of the board nor backside foil, since the feedthroughs and fiberglass of the board are not very thermally conductive. To obtain the best thermal resistance of the mounted part, θ_{JA}, the topside copper ground plane should have as much area as possible and be as thick as practical. If possible, the solder mask should be cut away from the EL1503 to improve thermal resistance. Finally, metal heatsinks can be placed against the board close to the part to draw heat toward the chassis.

Output Loading

While the drive amplifiers can output in excess of 500mA transiently, the internal metallization is not designed to carry more than 100mA of steady DC current and there is no current-limit mechanism. This allows safely driving rms sinusoidal currents of 2 x 100mA, or 200mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Power Supplies

The power supplies should be well bypassed close to the EL1503. A 3.3µF tantalum capacitor for each supply works well. Since the load currents are differential, they should not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no such ground loops will occur. This scheme is employed in the layout of the EL1503 demonstration board, and documentation can be obtained from the factory.

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency. The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (1dB peaking) for different supply voltages and gains:

TABLE 1. OPTIMUM DRIVER FEEDBACK RESISTOR FOR VARIOUS GAINS AND SUPPLY VOLTAGES

SUPPLY VOLTAGE	DRIVER VOLTAGE GAIN		
	2.5	5	10
±5V	2.7K	2.2K	2.0K
±12V	2.2K	2.0K	2.0K

Power Control Function

The EL1503 contains two forms of power control operation. Two digital inputs, C_0 and C_1, can be used to control the supply current of the EL1503 drive amplifiers. As the supply current is reduced, the EL1503 will start to exhibit slightly higher levels of distortion and the frequency response will be limited. The 4 power modes of the EL1503 are set up as shown in the table below:

TABLE 2. POWER MODES OF THE EL1503

C_1	C_0	OPERATION
0	0	I_S Full Power Mode (C_O or C_P)
0	1	2/3 I_S Power Mode (C_O or C_P)
1	0	1/3 I_S Terminate only mode
1	1	Power down

Another method for controlling the power consumption of the EL1503 is to connect a resistor from the I_{ADJ} pin to ground. When this pin is grounded (the normal state), the supply current per channel is as per the specifications table on page 2. When a resistor is inserted, the supply current is scaled according to the "I_S vs R_{SET}" graphs on page 10 in the Performance Curves section.

Both methods of power control can be used simultaneously. In this case, positive and negative supply currents (per amp) are given by the equations below:

$$I_S+ = 1mA + (\overline{C_1} \times 2/3) \times \frac{12.5mA}{(1 + R_{SET} \div 1k)} + (\overline{C_0} \times 1/3) \times \frac{12.5mA}{(1 + R_{SET} \div 1k)}$$

$$I_S- = 0 + (\overline{C_1} \times 2/3) \times \frac{12.5mA}{(1 + R_{SET} \div 1k)} + (\overline{C_0} \times 1/3) \times \frac{12.5mA}{(1 + R_{SET} \div 1k)}$$