Features

- Modulation Formats: BPSK, QPSK, SQPSK, 8-PSK, FM, FSK
- Symbol Rates: To 22.5MSPS (4 Samples/Symbol)
- Programmable: Reconfigurable to Data Rate, Modulation Format, and Order/Type of Tracking Loop
- Digital: Repeatable Performance Over Temperature and Time
- High Performance Reception: Bit Error Rate Approaches Less Than 0.5dB From Theory

| TABLE 1. INTERSIL DSP PRODUCTS FOR HIGH RATE DIGITAL RADIO RECEIVERS |
|-----------------|------------------|
| FUNCTIONAL BLOCK | INTERSIL PART     |
| VCA             | Analog Discrete  |
| 140MHz Quadrature Output | HI3086JCQ, CXA3086Q |
| 6-Bit A/D Converter (8-Bit A/D Converter) | (HI3026JCQ, HI3026AJCQ) |
| Decimating Filter | HSP43216 Halfband Filter |
| Digital DownConverter | HSP50110 Digital Quadrature Tuner |
| Matched Filter | HSP43168 Dual FIR Filter |
| Carrier and Symbol Tracking Loops | HSP50210 Digital Costas Loop |
| AGC Loop Filter | Analog Discrete |

**FIGURE 1. BLOCK DIAGRAM OF A HIGH RATE DIGITAL RADIO RECEIVER**
Introduction
The present HSP50110/210EVAL Board provides capabilities for evaluating received modulated signals with symbol rates up to 2.5MSPS. This high end limit on symbol rate is based on 20 samples per symbol. Many applications do not require such a large number of samples per symbol, and can still use the HSP50110/210EVAL Evaluation Board to breadboard and test these applications. Two limitations come into play as higher rates are implemented with this Evaluation Board:

1. The Serial FIR Filter maximum clock rate is (45MHz/10 bits) = 4.5MHz.
2. The transport delay, or propagation delay in the loop causing loop instability for input rates above 4.5MHz.

It is these limitations that prompts the presentation of a high symbol rate receiver implementation using the HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL) chip set. Figure 1 illustrates a high rate receiver configuration using the DQT and DCL demod parts. This implementation will be offered as the design solution, after the design considerations and trades have been presented.

High Rate Design Concerns
The primary limitations on a high speed design are the maximum operating speed of the digital parts and the bandwidth and resolution on the A/D converter. These key parameters are listed for the parts that will be configured for our high rate receiver design.

Maximum Clock Speed of HSP43216: 52MHz
Maximum Clock Speed of HSP50110: 52MHz
Maximum Clock Speed of HSP43168: 45MHz
Maximum Quadrature A/D
Conversion Speed: 140MSPS with 6 Bits
120MSPS with 8 Bits
Minimum Number Samples per Symbol: 4 Samples/Symbol

Selecting An A/D Converter
The design begins with selecting a high speed, wide bandwidth, high resolution D/A converter. Devices exist that output dual demultiplexed data samples at half the symbol rate. This relaxes the maximum clock rate of the following devices by 2. Such a device is the HI3086JCQ Intersil A/D. It is a 6-bit 140MSPS Flash A/D Converter with quadrature output samples. (The HI3026 A/D, an 8-bit 120MSPS device with dual demultiplexed output is also a design candidate). Subsequent DSP parts could operate up to a 70MHz maximum clock rate if the HI3086 is used.

Selecting The DSP Sample Rate
The Clock Rate Criterion
Selecting 4 samples per symbol yields the desired bandwidth. This sets the rate at which the HSP50110 Digital Quadrature Tuner will output symbol data. We can construct a DSP processing chain from this baseline symbol rate. The clock rate of the IF signal into the HSP50110 Digital Quadrature Tuner is set to be four times the symbol rate. By using an HSP43216 Halfband Filter in the Downconvert and Decimate mode (INT/EXT# = 0), the dual channel demultiplexed sampled data from the A/D can be input at four times the symbol rate. By noting that the A/D outputs 2 synchronous samples at half the A/D sample clock rate, the A/D sample rate is effectively four times the symbol rate.

The Re-Sampler in the DQT eliminates the need for the sample clock and the symbol rate to be exact integer related. (An even integer is used as an example for clarity and to yield a “ball park” solution for applications with non integer relationships). Note that an external NCO is used to drive the A/D clock port. This minimizes the clocking jitter in the system. Use of the DQT Re-Sample NCO in addition to a separate clock generator for the A/D and halfband will inherently have more jitter than the configuration shown. The DQT is used in the complex input mode.

Determining the DSP System Limiting Rate
The next limiting clock DSP element is the Halfband Filter which has a maximum clock rate at 52MHz. The rate through this decimating filter part can be optimized by using it in the Downconvert and Decimate Mode (INT/EXT# = 0). This allows dual (demultiplexed) inputs at the maximum clock rate. This sets the maximum system sustainable clock rate at the output of the A/D converter at 52MHz per data stream. The maximum system sustainable A/D input sample clock becomes twice the A/D output clock, or 104MHz. The decimate by two HalfBand filter output becomes a quadrature data stream at 52MHz and the symbol rate is one half of this, or 26MHz (2 samples on I, 2 samples on Q = 4 samples per symbol).

System Design Considerations
Frequency Domain Considerations for the A/D Sample Rate
Determining the appropriate A/D sample rate, requires more than just consideration of the clocking criterion of the DSP parts. The frequency plan of the receive system must complement the digitizing hardware and not produce alias components that will impede the ability to recover the signal of interest. Thus it is equally important that the sample rate be selected in a location relative to the IF signal, in a way that will not cause alias signals to fall in band. Many applications use undersampling techniques to recover signals from IF carriers by locating a harmonic of the sample frequency at a strategic distance from the IF signal. An alias of the high frequency IF carrier is then processed by the DSP hardware.

Figure 2A and 2B illustrate two examples of how a 90MHz A/D sample clock can be used to downconvert and process modulated IF signals. Figure 2A shows an oversampled 20MHz IF, while Figure 2B shows an undersampled 160MHz IF.

Figure 3 illustrates the spectral development at several points in the data path in the Block Diagram, from IF input to baseband output. The example has fS' = fS/2 (Decimate by 2) in the HBF and fS" = fS'/8 (Decimate by 8) in the DCL.
Additionally, it is insufficient to just consider the signals of interest. Those signals that fall in the band of the A/D converter must be removed by any anti-aliasing filters ahead of the A/D converter. These in-band signals, if not filtered out, will also alias around the clock frequency and may appear directly on top of the signal of interest. In example B of Figure 2, a 70MHz signal will interfere in such a way. The anti alias filter should be designed to attenuate the undesired signals to the point that it prevents such signal degradation. Note that an important system trade is the implementation of the anti-alias filter and the selection of the A/D clock frequency.
Implementation of a High Rate Radio Receiver

FIGURE 3. HIGH RATE RECEIVER SPECTRAL DEVELOPMENT

NOTE: $f_s = 2f_s' = 16f_s''$
**Matched Baseband Filter Requirements**

The final receiver design consideration is the construction of a matched baseband filter for the received signal. The DQT/DCL chipset offers two filters integral to the chip: 1) Integrate and Dump and 2) Square Root of Raised Cosine $\alpha = 0.4$. If one of these filters meets your system performance requirements, then no further design is required.

If your application requires a different filter, the HSP43168 or the HSP43124 can be inserted between the DQT and the DCL. The serial I/O filter (HSP43124) is limited to CLK = (45MHz/bit width). The Dual FIR filter (HSP43168) is limited to CLK = 45MHz. These parts may become the limiting factor for the maximum clock speed. This translates to an A/D sample rate at 90MHz, an A/D dual demultiplexed data output rate of 45MHz, a Halfband Filter dual data Output Rate of 45MHz, and a symbol rate of 22.5MHz. In general, filtering requirements may demand that greater than eight taps be used in the filter, and two HSP43168 chips may be required (one for I, one for Q) for adequate shaping.

**Summary**

Figure 1 outlines the implementation of the high symbol rate receiver. The solution assumes the need for an application specific matched filter, limiting the symbol rate to 22.5MHz. Key elements of the design are: the anti-alias filter, the quadrature output A/D converter, the dual input decimating Halfband Filter, the Digital Quadrature Tuner and the Digital Costas loop. The design uses the level detection feature of the HSP50110 to drive a Voltage Controlled Attenuator to keep the level at the converter input at an optimum value.

For information relative to setting the internal PLL parameters in the DQT/DCL chipset, refer to the HSP50110/210 EVAL Users Manual.
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third-parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   “Standard” - Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   “High Quality” - Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics product, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations, etc.), or may cause serious property damage (space systems; underground repowers; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failures at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics product, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to, redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics products” means any product developed or manufactured by or for Renesas Electronics.