**Introduction**

The following text describes the basic test procedures that can be used for most Intersil Op Amps. Note that all measurement conversions have been taken into account in the equations stated.

1. **Offset Voltage**
   The offset voltage ($V_{IO}$) of the amplifier under test (AUT) is measured via Test Circuit 1 as follows:
   
   1. Set $V+$ and $V-$ supplies to values specified in Table 1, Column (1) and $V_{DC}$ to 0V.
   2. Close $S_1$ and $S_2$, open $S_3$.
   4. Measure voltage at $E$ in volts (label as $E_1$).
   
   \[
   V_{IO} = \frac{E_1}{100} \text{ (mV) for } R_F = 50K, \quad V_{IO} = \frac{E_1}{10} \text{ (µV) for } R_F = 5M
   \]

   The gain of this circuit with $R_F = 50K$ ($R_F = 5M$) requires the output to be driven to 1000 (100,000) times the offset voltage necessary to maintain the output of the AUT at 0V. Note that the AUT output is always identical to $V_{DC}$. Overall circuit stability is maintained by the adjustable feedback capacitor $C_A$.

2. **Input Bias Current**
   The bias current flowing in or out of the positive terminal of the AUT ($I_{B+}$) is obtained using Test Circuit 1 by:
   
   1. Measuring $E_1$ as in procedure 1 (use $R_S = 100K$ for JFET input devices).
   2. Maintain $V_{DC}$ at 0V.
   3. Close $S_2$, open $S_1$ and $S_3$.
   4. Measuring voltage at $E$ in volts (label as $E_2$).
   
   \[
   I_{B+} = \frac{(E_1 - E_2) \times 100}{100} \text{ (nA) for } R_F = 50K, R_S = 10K, \quad I_{B+} = \frac{(E_1 - E_2) \times 10}{100} \text{ (nA) for } R_F = 5K, R_S = 100K
   \]

   The bias current flowing in or out of the negative terminal ($I_{B-}$) is found by:
   
   1. Following steps 1 and 2 for $I_{B+}$.
   2. Close $S_1$, open $S_2$ and $S_3$.
   3. Measuring voltage at $E$ in volts (label as $E_3$).
   
   \[
   I_{B-} = \frac{(E_1 - E_3) \times 100}{100} \text{ (nA) for } R_F = 50K, R_S = 10K, \quad I_{B-} = \frac{(E_1 - E_3) \times 10}{100} \text{ (nA) for } R_F = 5K, R_S = 100K
   \]

3. **Input Offset Current**
   Using Test Circuit 1, the input offset current ($I_{IO}$) of the AUT is determined by:
   
   1. Measuring $E_1$ as in procedure 1.
   2. Maintaining $V_{DC}$ at 0V.
   3. Open $S_1$, $S_2$ and $S_3$.
   4. Measuring voltage at $E$ in volts (label as $E_4$).
   
   \[
   I_{IO} = \frac{(E_1 - E_4) \times 100}{100} \text{ (nA) for } R_F = 50K, R_S = 10K, \quad I_{IO} = \frac{(E_1 - E_4) \times 10}{100} \text{ (nA) for } R_F = 50K, R_S = 100K
   \]

4. **Power Supply Rejection Ratio**
   Both positive and negative PSRRs are measured via Test Circuit 1. For PSRR+:
   
   1. Close $S_1$ and $S_2$, open $S_3$.
   2. Choose: $R_F = 50K$
   3. Set $V_{DC} = 0$, $V_+ = 10V$, and $V_- = -15V$.
   4. Measure voltage at $E$ in volts (label as $E_5$).
   5. Change $V_+$ to +20V.
   6. Measure voltage at $E$ in volts (label as $E_6$).

   \[
   \text{PSRR} + = 20 \log_{10} \left( \frac{10^{-4}}{E_5 - E_6} \right) \text{ (dB) for } R_F = 50K
   \]

   Similarly for PSRR-:
   
   1. Follow steps 1 and 2 for PSRR+ above.
   2. Set $V_{DC} = 0V$, $V_+ = +15V$, and $V_- = -10$.
   3. Measure voltage at $E$ in volts (label as $E_7$).
   4. Change $V_-$ to -20V.
   5. Measure voltage at $E$ in volts (label as $E_8$).

   \[
   \text{PSRR} - = 20 \log_{10} \left( \frac{10^{-4}}{E_7 - E_8} \right) \text{ (dB) for } R_F = 50K
   \]

5. **Common Mode Rejection Ratio**
   The CMRR is determined by adjusting Test Circuit 1 as follows:
   
   1. Close $S_1$ and $S_2$, open $S_3$.
   2. Choose: $R_F = 50K$
   3. Set $V_+ = +5V$, $V_- = -25V$, and $V_{DC} = -10V$.
   4. Measure voltage at $E$ in volts (label as $E_9$).
   5. Set $V_+ = 25V$, $V_- = -5V$, and $V_{DC} = 10V$.
   6. Measure voltage at $E$ in volts (label as $E_{10}$).

   \[
   \text{CMRR} = 20 \log_{10} \left( \frac{2 \times 10^{-4}}{E_9 - E_{10}} \right) \text{ (dB) for } R_F = 50K
   \]

6. **Output Voltage Swing**
   Test Circuit 2 is adjusted to measure $V_{OUT+}$ and $V_{OUT-}$; the procedure is:
   
   1. Select appropriate $V_+$ and $V_-$ supply values from Table 1, Column 1.
   2. Select specified $R_L$ from Table 1, Column 2.
3. Set $V_{IN} = 0.5V$.
4. Measure voltage at E in volts. $V_{OUT+} = E (V)$
   Similarly $V_{OUT-}$ is found by:
   1. Selecting specified $R_L$ from Table 1, Column 1.
   2. Setting $V_{IN} = -0.5V$.

7. Output Current

The output current corresponding to the output voltage of procedure 6 is found by:

1. Measuring $V_{OUT-}$ and $V_{OUT+}$ as in procedure 6.
   $$I_{OUT} = \frac{V_{OUT+}}{R_L} \text{ where } R_L \text{ is from Table 1, Column 2.}$$
   $$I_{OUT} = \frac{V_{OUT-}}{R_L} \text{ where } R_L \text{ is from Table 1, Column 2.}$$

8. Open Loop Gain

Both positive ($A_{VOL+}$) and negative ($A_{VOL-}$) open loop gain measurements are determined by adjusting Test Circuit 1.

For $A_{VOL+}$:
1. Close $S_1$, $S_2$ and $S_3$.
2. Select specified $R_L$ from Table 1, Column 3.
3. Set $R_F = 50K$.
4. Set $V_{DC} = 0V$, $V_+ = +15V$, and $V_- = -15V$.
5. Measure voltage at E in volts (label as $E_{13}$).
6. Set $V_{DC} = 10V$.
7. Measure voltage at E in volts (label as $E_{14}$).

$$A_{VOL+} = \frac{10}{E_{14} - E_{13}} \text{ (V/mV) for } R_F = 50K$$

For $A_{VOL-}$:
1. Follow steps 1, 2, 3, 4, and 5 above.
2. Set $V_{DC} = -10V$.
3. Measure voltage at E in volts (label as $E_{15}$).

$$A_{VOL-} = \frac{10}{E_{13} - E_{15}} \text{ (V/mV) for } R_F = 50K$$

9. Slew Rate

Test Circuit 3 is used for measurement of positive and negative slew rate. For SR+:
1. Select specified $R_L$, $A_{CL}$, and $C_L$ from Table 1, Columns 4, 5 and 6.
2. Apply a positive step voltage to $V_{AC}$ (refer to data book for test waveform).
3. Observe $\Delta V$ and $\Delta t$ at E. A standard approach is to use the 10% and 90% points or else the 25% and 75% points on the waveform.

$$SR^+ = \frac{\Delta V}{\Delta t}$$

For SR- repeat above procedure with negative input pulse.

$$SR^- = \frac{\Delta V}{\Delta t}$$

10. Full Power Bandwidth

Full power bandwidth is calculated by:
1. Measuring slew rate as above in procedure 9.
2. Measuring $V_{OUT+}$ as in procedure 6. (Typically $V_{OUT+}$ is assumed to be the guaranteed minimum $V_{OUT}$, usually 10V.)

$$FPBW = \frac{SR^+}{2\pi V_{OUT(PEAK)}}$$

11. Rise Time, Fall Time and Overshoot

The small signal step response of the AUT is determined via Test Circuit 3. The procedure requires:
1. Selecting the appropriate $R_L$, $A_{CL}$, and $C_L$ from Table 1, Columns 4, 5 and 6.
2. Applying a positive input step voltage for rise time $t_R$ and positive overshoot $OS^+$.
   Applying a negative input step voltage for fall time $t_F$ and negative overshoot $OS^-$. (Refer to data book for input waveforms.)
3. Observe output of AUT noting the key points as shown.
12. Settling Time
Test Circuit 6 is appropriate for settling time (tS) measurement, the procedure is:
1. Select R1 and R2 such that AUT is at the A_CL stated in Table 1, Column 5.
2. Select R3 and R4 so that R3 ≥ 2R1 and R4 ≥ 2R2 with the condition that the ratio
   \[
   \frac{R3}{R4} = \frac{R1}{R2}
   \]
   must be maintained.
3. Apply step voltage as specified in data book.
4. Measure the time from t1 (time input step applied) to t2 (the time ES settles to within a specified percentage of V_OUT - see data book). tS = t2 - t1
NOTE: Clipping diodes of Test Circuit 6 prevent overdrive of oscilloscope. (Recommend fast Schottky diodes.)

13. Gain Bandwidth Product
Test Circuit 4 is used for measuring GBP. The procedure is:
1. Sweep VIN thru the required frequency range.
2. With a network analyzer view gain (dB) versus frequency as below.
   \[
   A_V = \frac{V_{FINAL} - V_{FINAL}}{V_{FINAL}} \times 100\%
   \]
3. At the voltage gain of interest (AV) determine the corresponding frequency fC. Note that chosen AV must be greater than or equal to that stated in column 5 of Table 1.
   GBP = A_V x fC (Hz) where A_V is in V/V.

14. Phase Margin (Network Analyzer Method)
Test Circuit 4 is used to obtain phase margin measurement. The procedure is:
1. Sweep VIN thru the required frequency range.
2. Display gain in dB and phase in degrees versus frequency on analyzer as shown.
   \[
   \text{Phase Margin} = 180^\circ - P_1^\circ
   \]
   At a gain of 0dB (if A_CL = 1 in Table 1, column 5), record frequency \( f_1 \) and corresponding phase \( P_1 \).

15. Input Noise Voltage
Test Circuit 5 is designed for measuring input noise voltage. Use of the Quantec Noise Analyzer is recommended to obtain measurements at 1Hz bandwidth around a specific center frequency. The procedure is:
1. Set RG = 0
2. Set circuit card to gain of 10.
3. Select measurement frequency of interest.
4. Record noise voltage (label as E_n1). Units are nV/√Hz.

16. Input Noise Current
Using Test Circuit 5, the input noise current is obtained by:
1. Measure E_n1 as above for the desired frequency of interest.
2. Adjust RG so that VO > 2E_n1 (label VO as E_n2).
   \[
   I_n = \sqrt{\frac{(E_{n2})^2 - (E_{n1})^2 - 4kT\cdot G}{R_G^2}}
   \]
   Where K = 1.38 x 10^-23 (Boltzmann's Constant)
   \( T = 300^\circ\text{C} \) (27^\circ\text{C})

17. Channel Separation (Crosstalk)
Test Circuit 7 is used to measure channel separation (CS). The procedure is as follows:
1. Apply VIN at the frequency of interest to input of channel 1.
2. Select RL from Table 1, column 4.
3. Measure VO1.
4. Measure VO2 of channel 2.
   \[
   CS = 20 \log_{10} \left( \frac{V_{O2}}{V_{O1}} \right) \text{dB}
   \]
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Test Circuits

TEST CIRCUIT 1

TEST CIRCUIT 2

TEST CIRCUIT 3

ACL = 1 + \( \frac{R_F}{R_I} \)

\( R_{L(EFF)} = (R_F + R_I)||R_L \)

TEST CIRCUIT 4

TEST CIRCUIT 5
Test Circuits (Continued)

**TEST CIRCUIT 6**

**TEST CIRCUIT 7**

- **CHANNEL 1 (INPUT CHANNEL)**
  - 100kΩ
  - VIN
  - VO1
  - AUT
  - V+ V-

- **CHANNEL 2 (LEAKAGE CHANNEL)**
  - 1kΩ
  - VIN
  - VO2
  - AUT
  - V+ V-
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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Mplils, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9351 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5H, UK
Tel: +44-1628-851-700, Fax: +44-1628-851-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 3001, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-9888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2266-6688, Fax: +852-2866-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shih North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9650, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bedemere Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Aircorp, Aircorp Trade Centre, No. 18, Jln Persiaran Barat, 46500 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +603-3-7955-930, Fax: +603-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3157, Fax: +82-2-558-5338

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