

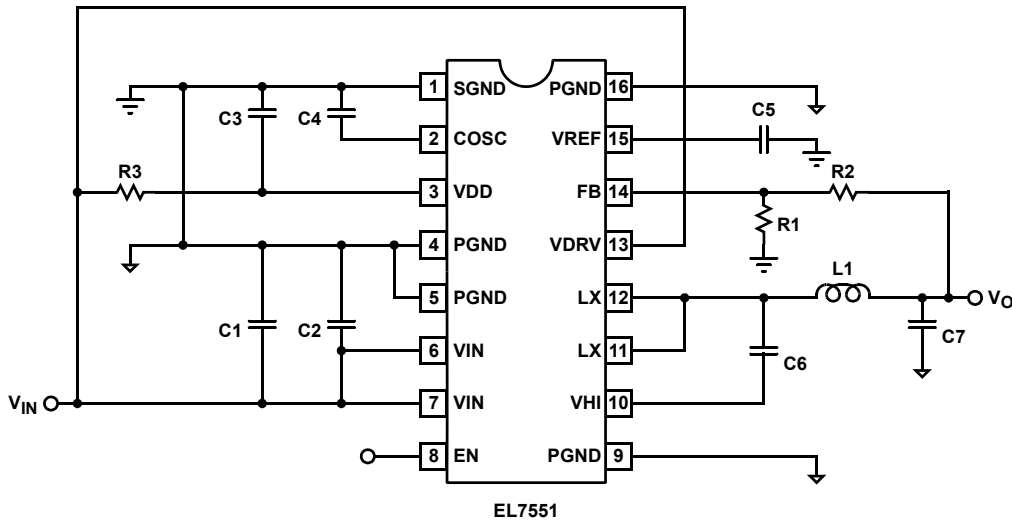
**NOT RECOMMENDED FOR NEW DESIGNS
SEE EL7531 OR EL7536**



The EL7551 is a Buck (Step Down) DC:DC controller with integrated synchronous MOSFETs in a 16-pin QSOP package. With very few external components, a 1A step-down DC:DC converter can be very easily built, resulting in saved board space (<math><0.5\text{in}^2</math>), minimal design effort, and improved design time.

This demo board is operated at about 500kHz switching frequency. The input voltage is from 4.5V to 5.5V. This document outlines the design consideration and lists the bill of materials and the layout. Please also refer to the advanced data sheet of EL7551 for detailed applications of the features.

EL7551 Demo Board Circuit Schematic



EL7551 Demo Board Bill of Material $V_{IN} = 5V, V_{OUT} = 3.3V$

REFERENCE DESIGNATION	VALUE	MANUFACTURER	MANUFACTURER'S PHONE NUMBER	PART NUMBER
C1	10 μ F	Panasonic	408-945-5660	ECJ-3YBOJ106K
C2, C3, C5, C6	0.1 μ F, 0603	Any		
C4	270pF, 5%, 0603	Any		
C7	47 μ F	Sprague	207-324-4140	293D476X00100D2W
L1	10 μ H	Coilcraft	847-639-6400	D01813P-103HC
R1	1k Ω , 0603	Any		
R2	2370 Ω , 0603	Any		
R3	39.2 Ω , 0603	Any		

Design Considerations

Choosing the Component Values

The following requirements are specified for a DC:DC converter:

- Input voltage range: $V_{IN} = 4.5V-5.5V$
- Output voltage: $V_O = 3.3V$
- Max output voltage ripple: $\Delta V_O = 50mV$
- Output max current: $I_O = 1A$

The following steps briefly outline the steps to choose components. For a detailed design discussion, please refer to Elantec Application #18 "Designing a High Efficiency DC:DC Converter with the EL75XX."

1. Choose the feedback resistor divider.

The output voltage is decided by:

$$V_O = 0.975 \times \left(1 + \frac{R_2}{R_1} \right)$$

2. Choose the converter switching frequency F_S .

F_S , inductor L_1 , output capacitor C_7 , and EL7551's switching loss are closely related. many iterations (or thermal measurements) may be required before a final value can be decided.

Please refer to the EL7551 data sheet for the F_S vs C_{OSC} curve.

3. Inductor L_1 .

The EL7551 is internally ramp-compensated. For optimal operation, the inductor current ripple should be less than 0.5A.

If $\Delta I_L = 0.5A$, then:

$$L = \frac{(1-D) \times V_O}{\Delta I_L \times F_S}$$

where:

$$D = \frac{V_O}{V_{IN}}$$

Choosing $L_1 = 10\mu H$ yields $\Delta I_{LMAX} = 0.26A$ and $\Delta I_{LMIN} = 0.18A$. L_1 should also be able to handle DC current of 1A and peak current of 1.2A at temperature range.

4. Output capacitor C_7 .

ΔV_O and ΔI_L normally decide C_7 value. ΔV_O requires ESR of C_7 be less than:

$$ESR = \frac{\Delta V_O}{\Delta I_{LMAX}} = 136m\Omega$$

Double-check the RMS current requirement of the output capacitor:

$$\Delta I_{C7} = \frac{\Delta I_{LMAX}}{\sqrt{12}}$$

which is 0.11A. For a capacitor or combination of capacitors with 136m Ω parallel ESR, it is more than enough to handle this current.

5. Input capacitor C_1 .

If all the AC current is handled by the input capacitor C_1 , its RMS current is calculated as:

$$I_{IN,rms} = \sqrt{[D \times (1-D)]} \times I_O$$

This gives almost 0.5A when $D = D_{MAX}$. Therefore a cap with 0.5A current handling capability should be chosen. However, in case some other capacitor is sharing current with it, C_1 's current requirement can be reduced.

Layout Considerations

The layout is very important for the converter to function properly. Power Ground (\downarrow) and Signal Ground (∇) should be separated to ensure that the high pulse current in the Power Ground never interferes with the sensitive signals connected to Signal Ground. They should only be connected at one point (normally at the negative side of either the input or output capacitor.)

The trace connected to pin 14 (FB) is the most sensitive trace. It needs to be as short as possible and in a "quiet" place, preferably between the PGND and SGND traces.

In addition, the bypass capacitor C_3 should be as close to pins 1 and 3 as possible.

The heat of the chip is mainly dissipated through the PGND pins. Maximizing the copper area around these pins is preferable. In addition, a solid ground plane is always helpful for the EMI performance.

Demo Board Layout

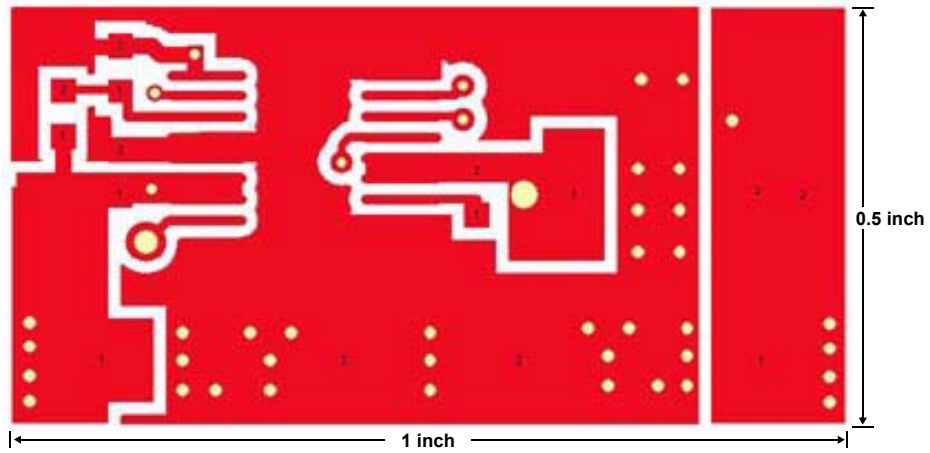


FIGURE 1. TOP LAYER

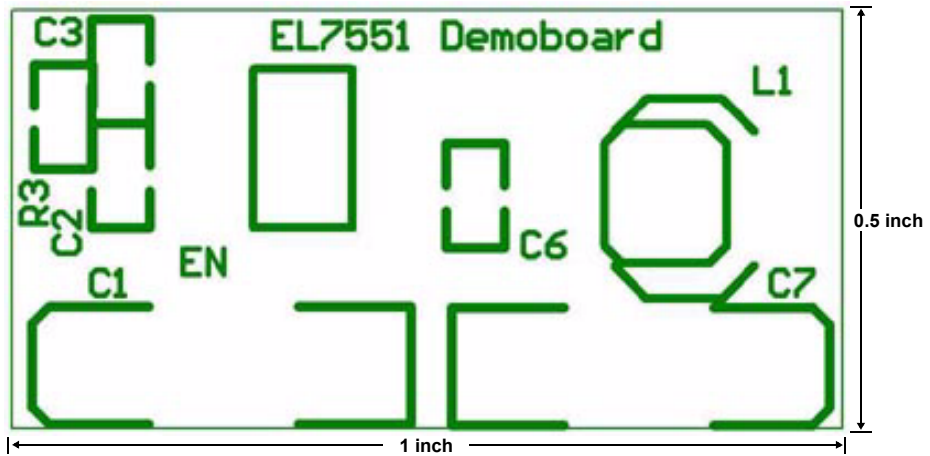


FIGURE 2. TOP SILKSCREEN

Demo Board Layout (Continued)

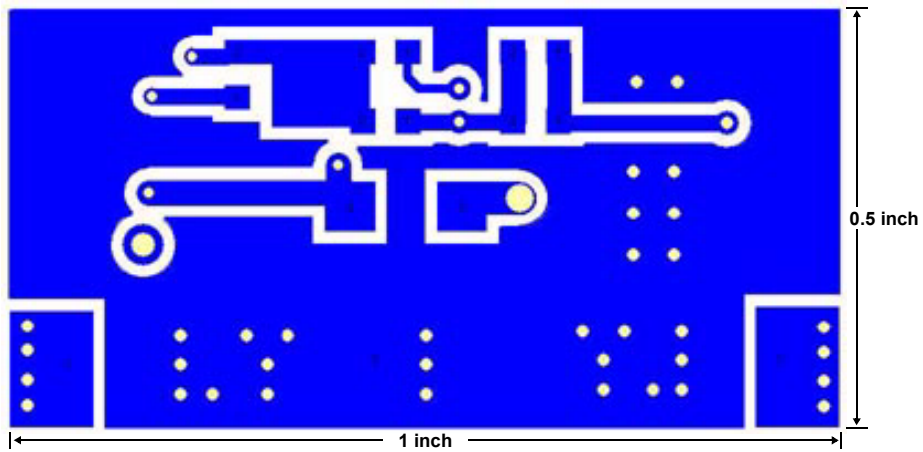


FIGURE 3. BOTTOM LAYER

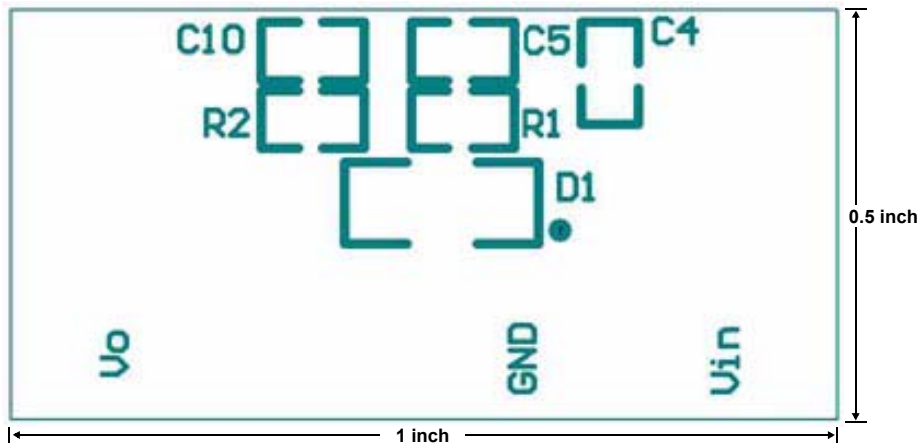


FIGURE 4. BOTTOM SILKSCREEN

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