

**Introduction**



The EL7564 is a full featured Buck (Step Down) DC:DC controller with integrated synchronous MOSFETs.

With very few external components, a 4A step-down DC:DC converter can be very easily built, resulting in saved board space, minimal design effort, and improved design time.

This demo board is operated at about 350kHz switching frequency. The input voltages are 4.5V to 5.5V. This document outlines the design consideration and lists the bill of materials and the layout. Please also refer to the advanced data sheet of EL7564 for detailed applications of the features.

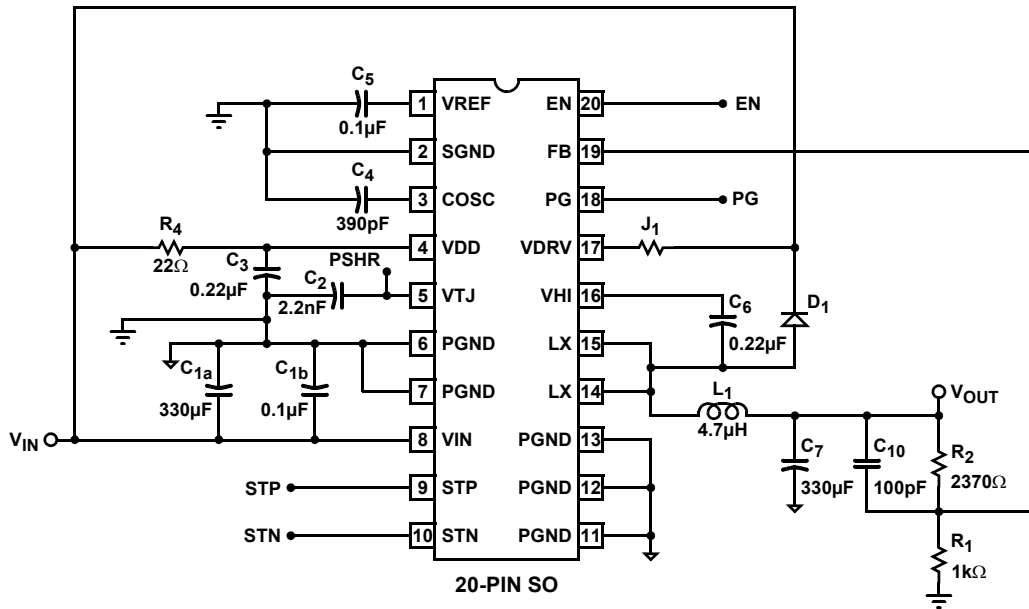


FIGURE 1. EL7564CM DEMO BOARD CIRCUIT SCHEMATIC



## Design Considerations

### Choosing the Component Values

The following requirements are specified for a DC:DC converter:

Input voltage range:  $V_{IN} = 4.5V-5.5V$

Output voltage:  $V_O = 3.3V$

Max output voltage ripple:  $\Delta V_O = 50mV$

Output max current:  $I_O = 4A$

The following steps briefly outline the steps to choose components. For a detailed design discussion, please refer to Elantec Application #18 "Designing a High Efficiency DC:DC Converter with the EL75XX."

1. Choose the feedback resistor divider.

The output voltage is decided by:

$$\text{EL7564CM: } V_O = 0.975 \times \left(1 + \frac{R_2}{R_1}\right)$$

$$\text{EL7564CRE: } V_O = 0.992 \times \left(1 + \frac{R_2}{R_1}\right)$$

If  $R_1$  is chosen to be  $1k\Omega$ , then:

$$R_2 = 2.37k\Omega$$

2. Choose the converter switching frequency  $F_S$ .

$F_S$ , inductor  $L_1$ , output capacitor  $C_7$ , and EL7564's switching loss are closely related. many iterations (or thermal measurements) may be required before a final value can be decided.

Please refer to the EL7564 data sheet for the  $F_S$  vs  $C_{OSC}$  curve.

3. Inductor  $L_1$ .

The EL7564 is internally ramp-compensated. For optimal operation, the inductor current ripple range should be less than 0.8A.

If  $\Delta I_L = 0.8A$ , then:

$$L = \frac{(1-D) \times V_O}{\Delta I_L \times F_S}$$

when:

$$D = \frac{V_O}{V_{IN}}$$

Choosing  $L_1 = 4.7\mu H$  yields  $\Delta I_{LMAX} = 0.72$  and  $\Delta I_{LMIN} = 0.64A$ .  $L_1$  should also be able to handle DC current of 4A and peak current of 4.4A at temperature range.

4. Output capacitor  $C_7$ .

$\Delta V_O$  and  $\Delta I_L$  normally decide  $C_7$  value.  $\Delta V_O$  requires ESR of  $C_7$  be less than:

$$\text{ESR} = \frac{\Delta V_O}{\Delta I_{LMAX}} = 70m\Omega$$

Double-check the RMS current requirement of the output capacitor:

$$\Delta I_{C7} = \frac{\Delta I_{LMAX}}{\sqrt{12}}$$

which is 0.21A. For a capacitor or combination of capacitors with  $70m\Omega$  parallel ESR, it is more than enough to handle this current.

5. Input capacitor  $C_{1a}$ .

If all the AC current is handled by the input capacitor  $C_{1a}$ , its RMS current is calculated as:

$$I_{IN,rms} = \sqrt{[D \times (1-D)]} \times I_O$$

This gives almost 1.97A when  $D = D_{MAX}$ . Therefore a cap with 1.97A current handling capability should be chosen. However, in case some other capacitor is sharing current with it,  $C_{1a}$ 's current requirement can be reduced.

### **Layout Considerations**

The layout is very important for the converter to function properly. Power Ground (↓) and Signal Ground ( $\frac{\perp}{\perp}$ ) should be separated to ensure that the high pulse current in the Power Ground never interferes with the sensitive signals connected to Signal Ground. They should only be connected at one point (normally at the negative side of either the input or output capacitor.)

The trace connected to the FB pin is the most sensitive trace. It needs to be as short as possible and in a “quiet” place, preferably with the PGND or SGND traces surrounding it.

In addition, the bypass capacitor connected to the  $V_{DD}$  pin needs to be as close to the pin as possible.

The heat of the chip is mainly dissipated through the PGND pins for the CM package, and through the heat pad at the bottom for the CRE package. Maximizing the copper area around these PGND pins or the heat pad is preferable. In addition, a solid ground plane is always helpful for the EMI performance.

### **Performance**

The waveforms and thermal performance curves of this demo board are shown on the next pages. The junction temperature of the chip can be determined by:

$$T_J = 75 + \frac{1.2 + VT_J}{0.00384}$$

Typical Performance Curves

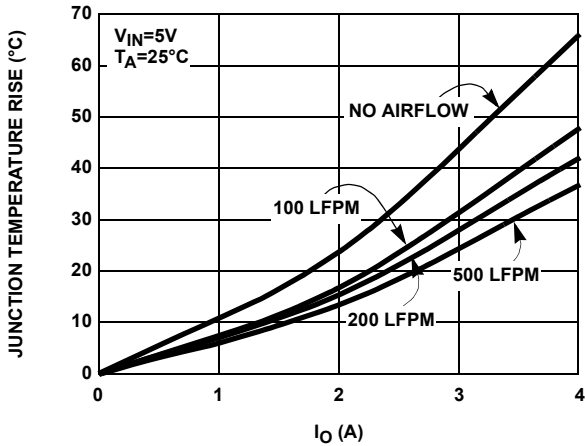


FIGURE 3. EL7564CM JUNCTION TEMPERATURE RISE ON DEMO BOARD

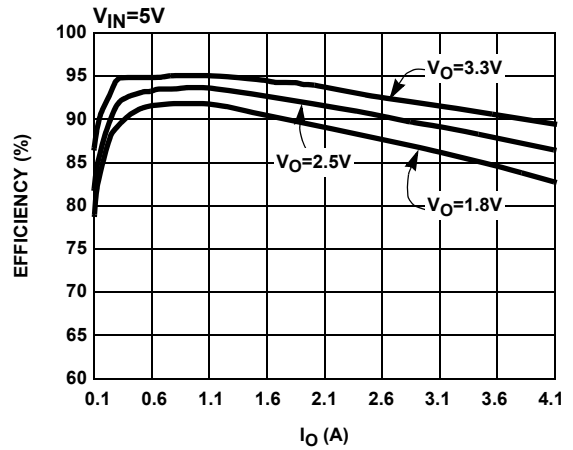


FIGURE 4. EL7564CRE EFFICIENCY

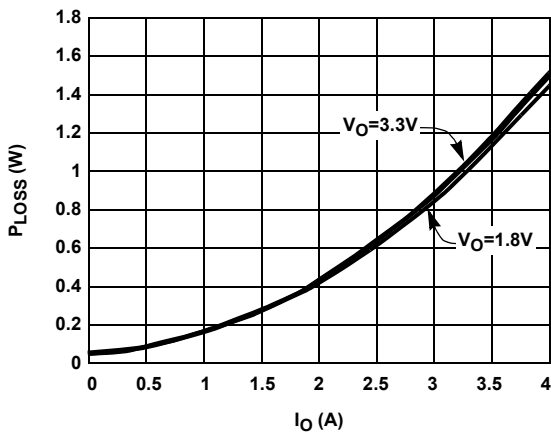


FIGURE 5. TOTAL CONVERTER POWER LOSS - EL7564CRE

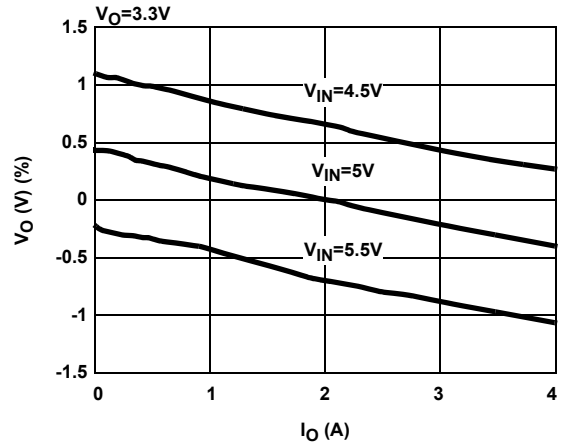


FIGURE 6. EL7564CRE LOAD REGULATION

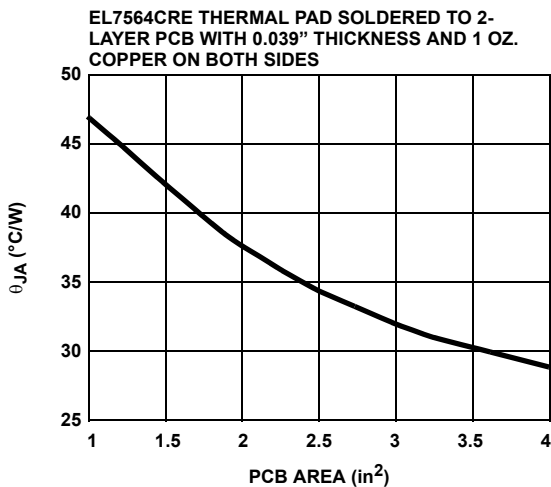


FIGURE 7. EL7564CRE THERMAL RESISTANCE VS PCB AREA - NO AIRFLOW

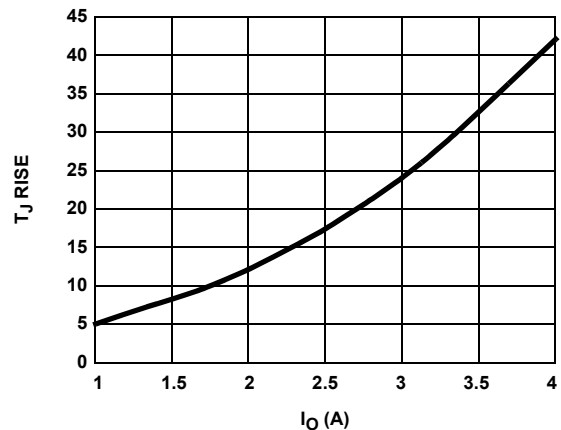


FIGURE 8. EL7564CRE JUNCTION TEMPERATURE RISE ON DEMO BOARD - NO AIRFLOW

Demo Board Waveforms

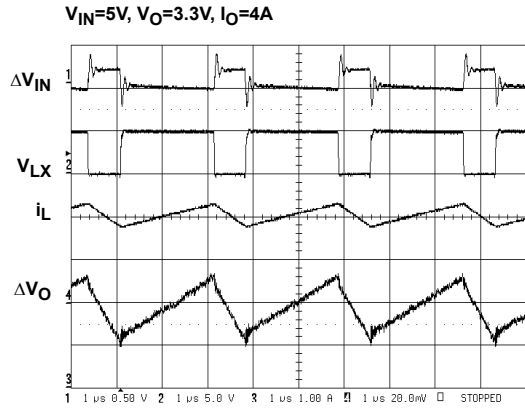


FIGURE 9. SWITCHING WAVEFORMS

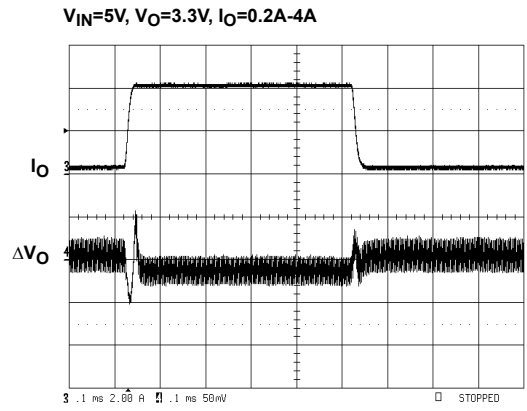


FIGURE 10. TRANSIENT RESPONSE

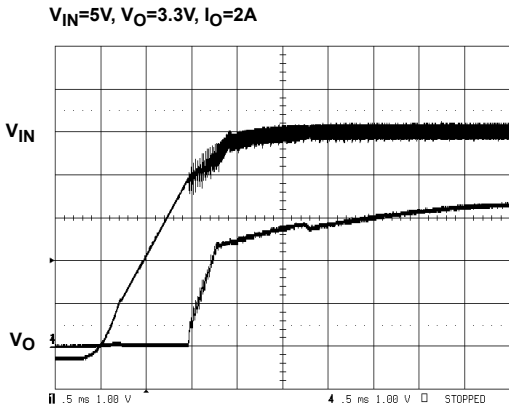


FIGURE 11. POWER-UP

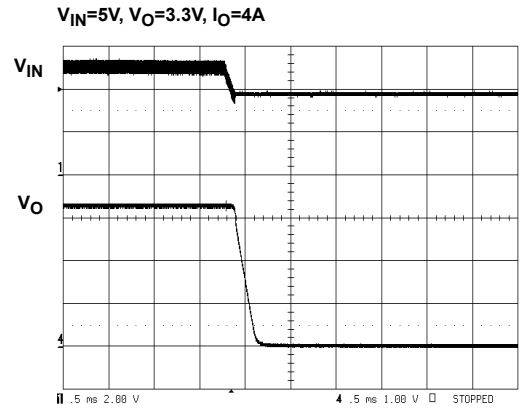


FIGURE 12. POWER-DOWN

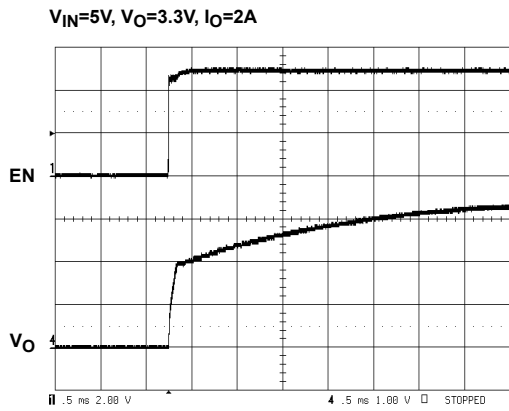


FIGURE 13. RELEASING EN

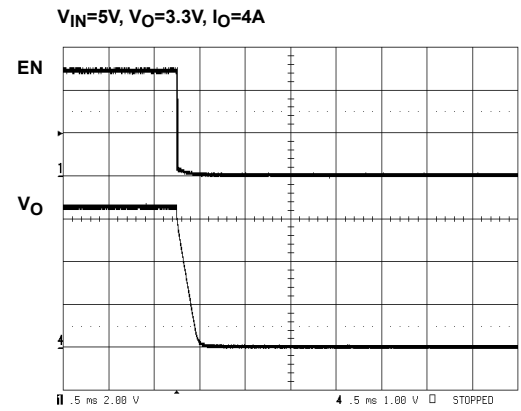


FIGURE 14. SHUT-DOWN

Demo Board Waveforms (Continued)

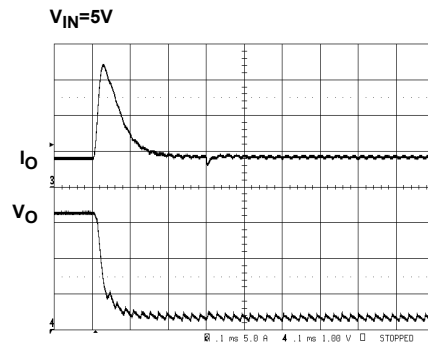


FIGURE 15. SHORT-CIRCUIT PROTECTION

Demo Board Layout (EL7564CM)

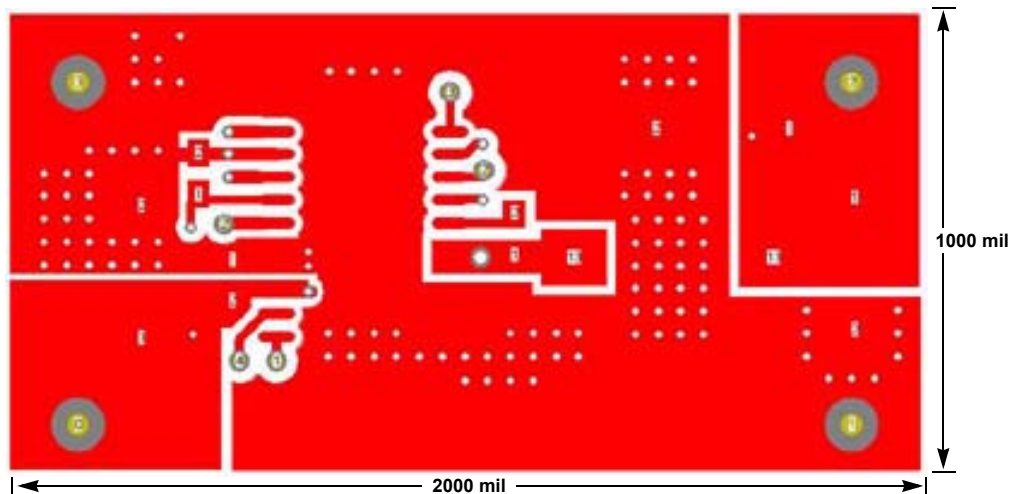


FIGURE 16. TOP LAYER

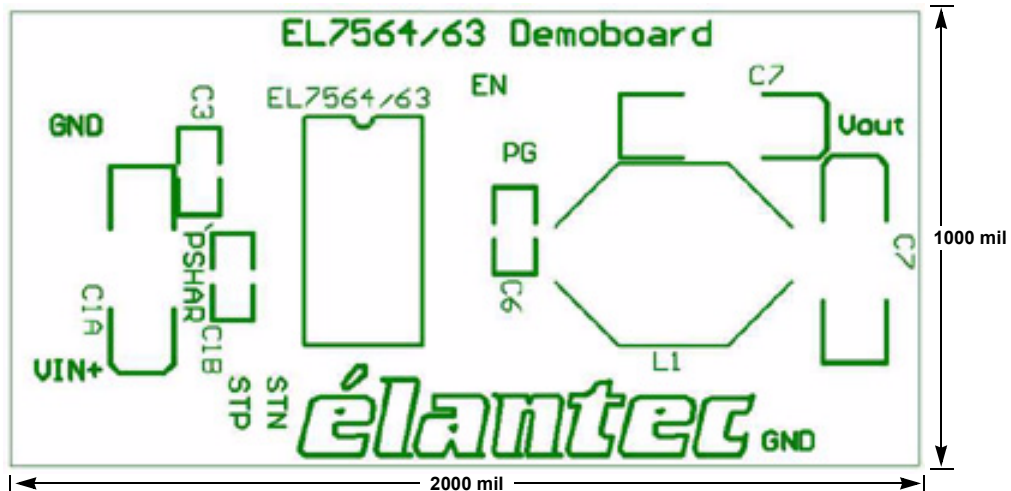


FIGURE 15. TOP SILKSCREEN

Demo Board Layout (EL7564CM) (Continued)

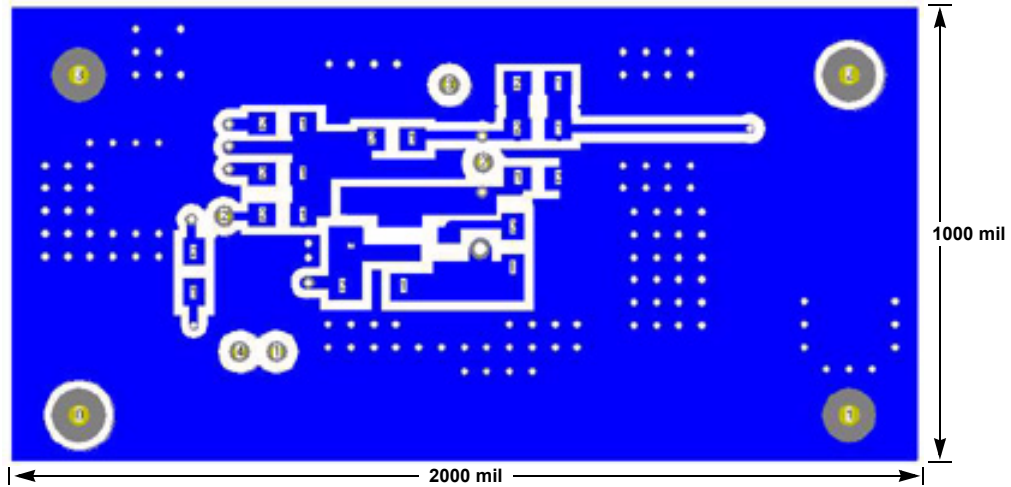


FIGURE 17. BOTTOM LAYER

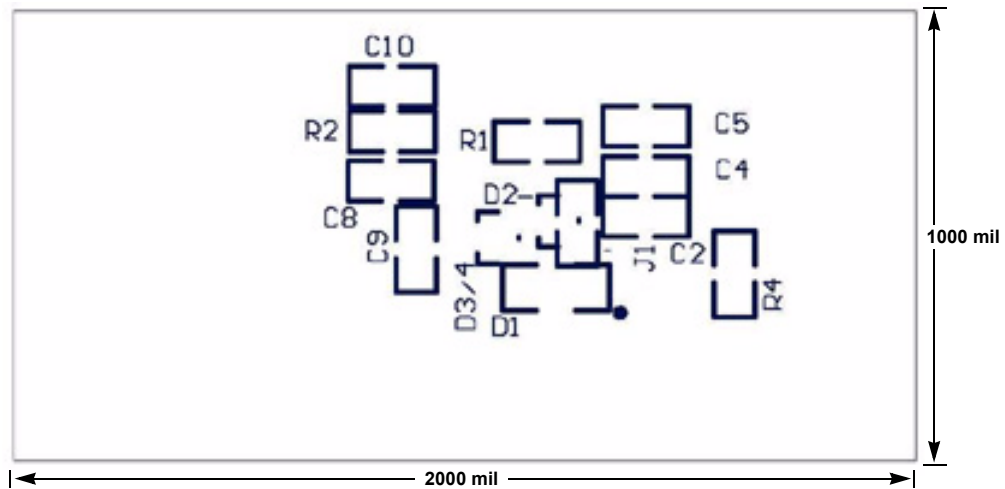


FIGURE 16. BOTTOM SILKSCREEN

Demo Board Layout (EL7564CRE) (Continued)

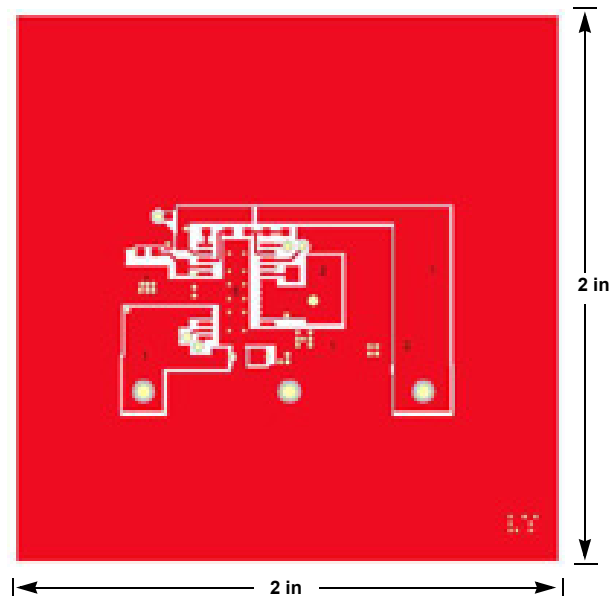


FIGURE 18. TOP LAYER

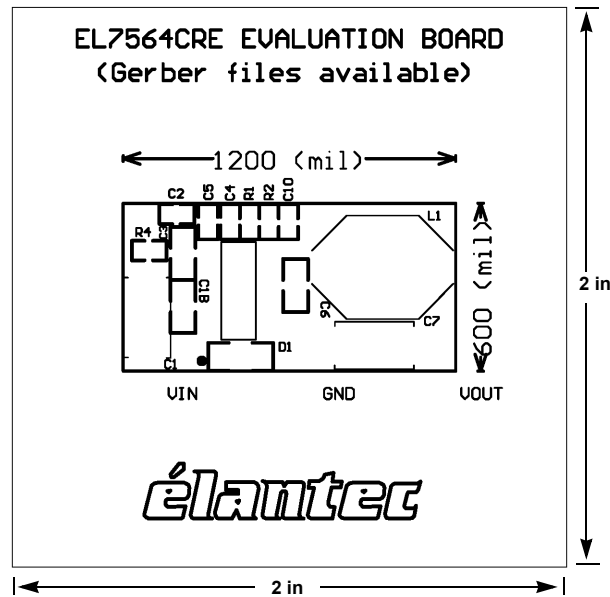


FIGURE 17. TOP SILKSCREEN

Demo Board Layout (EL7564CRE) (Continued)

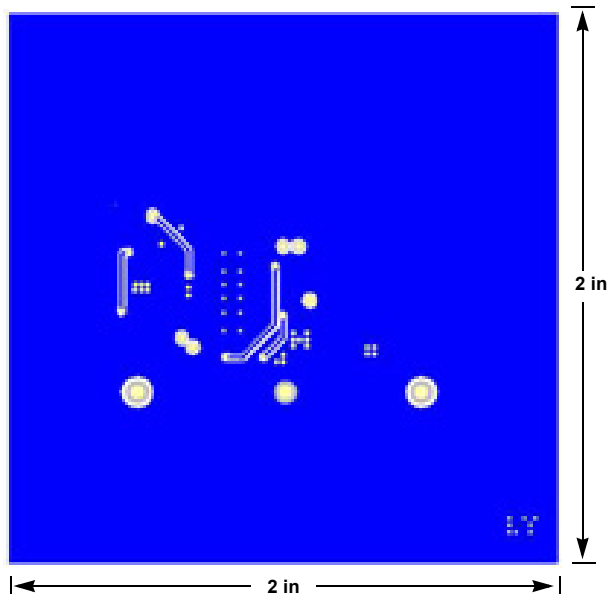


FIGURE 19. BOTTOM LAYER

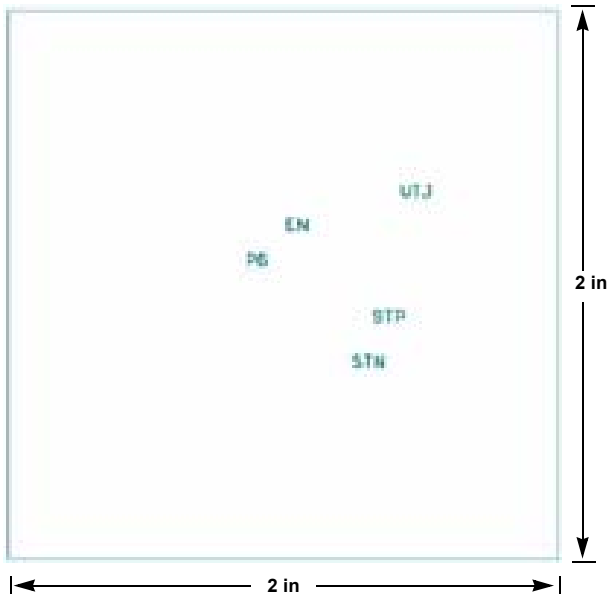


FIGURE 18. BOTTOM SILKSCREEN

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)