

Introduction

This Techbrief will illustrate the use of a dual SPST Switch in a multi-Phase PWM High current, high slew-rate power application. The ISL43120 enables the user to change the supply's output voltage via logic control. Typical application would be for testing of product at 10% high supplies as part of an outgoing inspection. The 3 phase power converter (Figure 2) shows the connection of the ISL43120 dual SPST switch. Single logic control is achieved by shorting the VIN₁ and VIN₂ pins of the ISL43120 together.

Operation

Figure 2 shows a simplified diagram of the voltage regulation and current control loops for a three-phase converter. The ISL6558 Precision Multi-Phase PWM Controller provides both voltage and current feedback to precisely regulate output voltage and tightly control phase currents of the three power channels.

Voltage Loop

Output voltage feedback is applied via the resistor combination of R_{FB} and R_{OS} to the inverting input of the error amplifier. The output voltage can now be changed to a predetermined value via logic control of the ISL43120. The output voltage with the parallel resistor R_P is calculated using Equation 1.

The process of determining the values of R_{FB} and R_{OS} first starts with Equation 2, or Equation 3 if output droop compensation is required. Once the values of R_{FB} and R_{OS} are determined, Equation 1 can be used to determine the output voltage as a function of the parallel combination of R_P and R_{OS}. Note: The value of R_P includes the switch resistance.

$$V_{OUT} = \frac{0.8V(R_{FB} + (R_{OS} \parallel R_P))}{R_{OS} \parallel R_P} \quad (\text{EQ. 1})$$

The output voltage, V_{OUT}, must be fed back to the VSEN pin separately from the feedback components to the FB pin. If VSEN and FB are tied together, the error amplifier will hold the VSEN voltage at the reference level while the actual output voltage level could be much different. This would mask the output voltage and prevent the protection features from reacting to undervoltage or overvoltage conditions at the proper time. It is for this reason, that the second SPST switch and the duplication of resistors R_{OS} and R_P are required as shown in Figure 2.

If the output voltage is required to be 0.8V, the user could then tie the output directly back to the VSEN pin without a resistor divider.

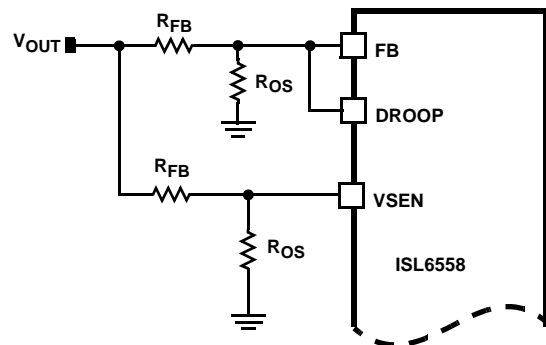


FIGURE 1. VSEN RESISTOR DIVIDER CONFIGURATION

Current Loop

The current control loop keeps the channel currents (IL₁, IL₂, IL₃) in balance. During the PWM off-time of each channel, the voltage developed across the r_{DS(ON)} of the lower MOSFET is sampled (Q₁, Q₂, Q₃) and fed back to a current sensing network. This signal keeps each channel's output current contribution balanced relative to the other active channels.

Reference the ISL6558 data sheet for further details of the internal operation of the ISL6558.

SELECTING R_{FB} AND R_{OS}

If output droop compensation is not required the DROOP pin must be left open. Simply select a value for R_{FB} and calculate R_{OS} based on the following equation:

$$R_{OS} = R_{FB} \times \frac{0.8V}{V_{OUT} - 0.8V} \quad (\text{EQ. 2})$$

Equation 1 can then be used to determine the output voltage as a function of R_p.

In applications where droop compensation is desired, tie the DROOP and FB pins together. Select R_{FB} first given the following equation, where V_{DROOP} is the desired amount of output voltage droop at full load. This equation is contingent upon the correct selection of the ISEN resistors discussed in the *Fault Protection* section of the data sheet.

$$R_{FB} = \frac{V_{DROOP}}{50\mu A} = 20 \times 10^3 \times V_{DROOP} \quad (\text{EQ. 3})$$

Calculate R_{OS} based on R_{FB} using the following equation. Where V_{OUT,NL} is the desired output voltage under no-load conditions.

$$R_{OS} = R_{FB} \times \frac{0.8V}{V_{OUT,NL} - 0.8V} \quad (\text{EQ. 4})$$

Typical Application - 3 Phase Converter

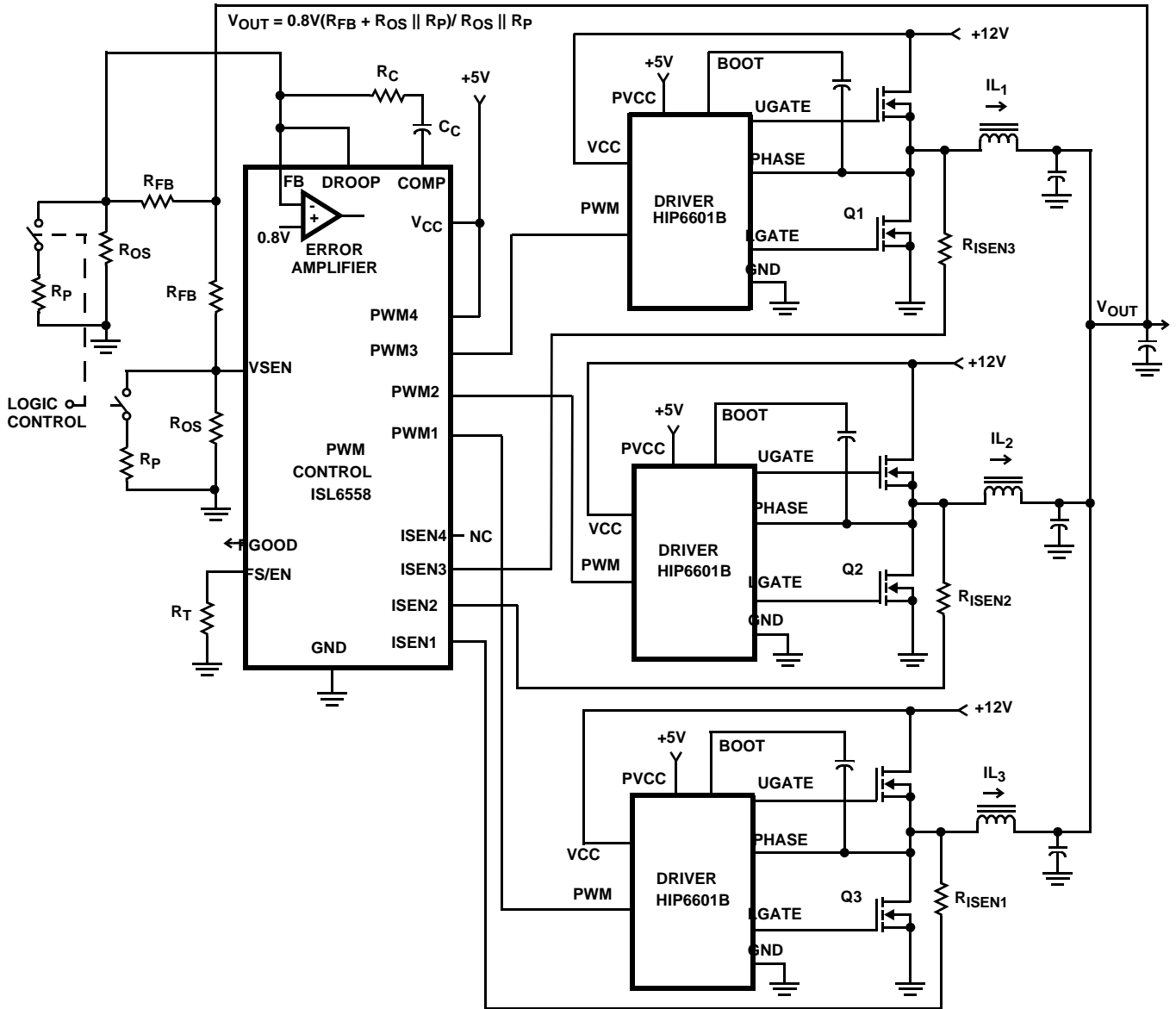


FIGURE 2. SCHEMATIC OF THE ISL6558 3 PHASE CONVERTER WITH VARIABLE OUTPUT VOLTAGE VIA LOGIC CONTROL

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