

Introduction

The HMP8156 is Intersil Corporation's first integrated digital NTSC/PAL encoder. In our continuing effort to improve our products, we have made several changes to the design to improve its performance and will be replacing the HMP8156 with the HMP8156A. This Tech Brief describes the differences between the two versions of the part.

The HMP8156A and HMP8154 encoders are based on the same design so this Tech Brief also describes all the differences between the HMP8156 and the HMP8154 except for the flicker filter. Please refer to the HMP8154/HMP8156A data sheet (FN4343.1) for information about the HMP8154's flicker filter.

The differences are limited to two main areas of the parts: the internal control registers and the digital to analog converters (DACs). The net result of the modifications is that the external RSET value changes. The sections below describe the differences in detail.

Control Register Changes

The internal control registers are used to program the part for different operating modes and to obtain status information from the part. They are written and read via the I2C bus.

Except for the read only product ID register, we implemented the changes so that following a hardware or software reset cycle, all of the added bits are programmed so that the HMP8156A operates the same way the HMP8156 would have. This minimizes the impact to existing systems.

Product ID

The product ID register is located at subaddress 0x0. The HMP8156 product ID returns the value 0x56 when read. On the HMP8156A, the value is 0x54.

Note: The product ID is 0x54 for the HMP8154 too. Even though both parts return the same product ID value, applications can still uniquely identify them using the video processing register bits. Please refer to TB352, *Identifying the HMP8154 and HMP8156A via the I2C Bus*.

Output Format

The output format register is located at subaddress 0x1. The HMP8156 data sheet states that composite with RGB output is not allowed for NTSC and (M, N, CN) PAL video timing standards. If RGB output was selected with one of these standards, the RGB output levels would not be correct. The HMP8156A generates correct levels for all standards and all output formats.

Video Processing

The video processing register is located at subaddress 0x3. For the HMP8156A, we assigned functions to several bits which were reserved in the HMP8156. The additional functions include a programmable blanking pedestal for RGB output format, programmable pin assignments for RGB output format, and the flicker filter. By default, all the new functions are programmed so the HMP8156A operates like the HMP8156.

Although all the flicker filter control bits are present in the HMP8156A, it ignores data writes to the flicker filter enable bit. This bit will always return a '0' when read. The other flicker filter control bits may be written with either value but they will have no effect unless the flicker filter itself is enabled. The flicker filter may only be enabled in the HMP8154.

Power Down Modes

The power down modes are controlled by bits in the host control register located at subaddress 0xF. The HMP8156 has two power down modes: total power down and one DAC disable (the NTSC/PAL 2 output). The HMP8156A provides additional control to individually disable the other three DACs as well. By default, both encoders power up or reset with all DACs enabled.

Field Timing

We added two additional control registers to the HMP8156A. They allow programmable timing relationships between the horizontal and vertical syncs when the syncs are inputs. The field timing control registers are located at subaddresses 0x26 and 0x27. The default values of the registers program the HMP8156A to operate like the HMP8156.

DAC Changes

We made design and layout changes to the encoder's DACs to improve their performance and manufacturability. The changes compensate for differences between wafer production runs and process induced gradients across each chip. The changes do not affect the basic functionality of the DACs.

Internal Reference Voltage

The DACs require a reference voltage which determines their full scale output current. The encoder provides an internal reference voltage, reducing the external components required. We made changes to the HMP8156A to reduce the reference voltage range. The internal reference voltage specifications for both parts are shown in Table 1.

TABLE 1. VREF OUTPUT VOLTAGE COMPARISON

DEVICE	MIN	TYP	MAX
HMP8156	1.13	1.23	1.32
HMP8156A	1.16	1.20	1.24

The changes also improved the power supply rejection ratio of the reference voltage and the DACs.

Fullscale Current Gain

The DAC reference voltage is converted into a reference current as shown in Figure 1. There is a gain factor from the reference current to the fullscale output current. We made changes to the circuit and its layout to reduce the range of gain values. The typical gain changed from 3.6 in the HMP8156 to 3.9 for the A version.

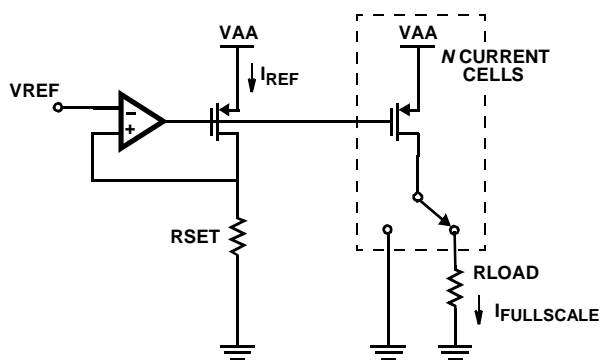


FIGURE 1. DAC VREF TO I_FULLSCALE CONVERSION

RSET Value

As a result of changes made to the internal voltage reference and the fullscale current gain, the external resistor which sets the fullscale output current must be changed as well. As shown in the data sheets, RSET is given by Equation 1:

$$RSET = GAIN \times VREF / I_{FULLSCALE} \quad (EQ. 1)$$

For the voltage reference and gain values shown above, and with a 37.5Ω net load, RSET changes from 124Ω with the original design to 133Ω for the HMP8156A. This is the most important difference between the designs.

If HMP8156A encoders are used in place of HMP8156 parts and the RSET resistor value is not changed, then the fullscale output current will be approximately 7% higher than it should be.

Linearity

We made several changes to the layout of the output current cells to improve the linearity of the HMP8156A. Typical plots of the integral nonlinearity error of the two encoder versions are shown in Figure 2.

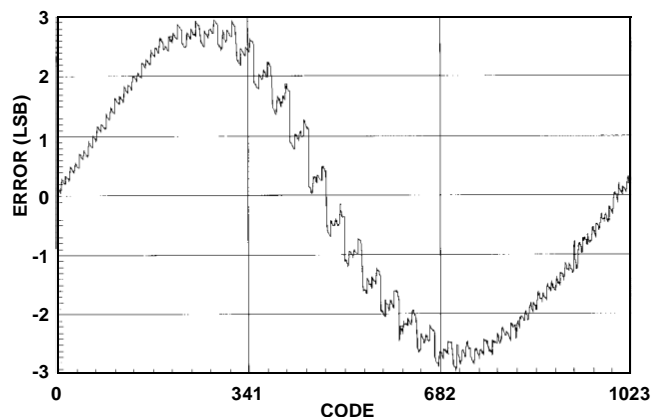


FIGURE 2A. HMP8156 DAC INTEGRAL NON-LINEARITY ERROR

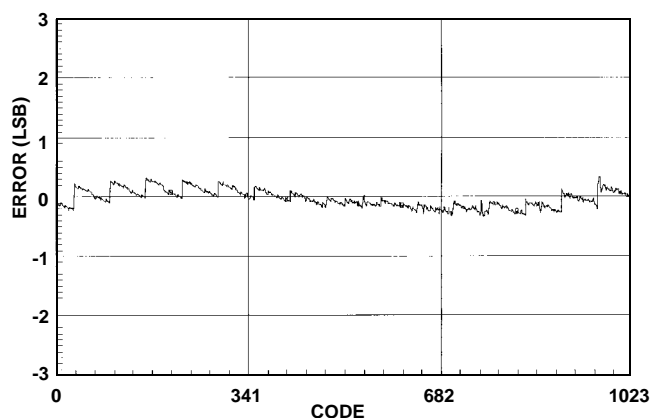


FIGURE 2B. HMP8156A DAC INTEGRAL NON-LINEARITY ERROR

External Compensation Capacitors

The addition of an internal compensation capacitor makes the second external compensation cap optional. To reduce the external part count, the 0.1μF capacitor connected to COMP2 (pin 63) may be deleted when the HMP8156A is used. However, keeping the COMP2 capacitor does not affect the A encoder's performance.

Summary

This Tech Brief has described the changes we made to add functionality and improve performance of the encoder. However, none of the changes for the HMP8156A significantly affect designs currently using the HMP8156.

The most important change to note is that the RSET resistor value must be adjusted to match the changes to the fullscale current gain and, if used, the internal reference voltage. For most applications, RSET changes from 124Ω to 133Ω.

For systems which use the product ID register, the software must be changed to expect 0x54 instead of 0x56.

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