

**Introduction**

The purpose of this tech brief is to update you on a temporary change to the clock requirements for the HI7188. The master system clock of the HI7188 can be supplied by either connecting a crystal between OSC<sub>1</sub> and OSC<sub>2</sub> pins as shown in Figure 1 or a CMOS compatible clock signal connected to the OSC<sub>1</sub> pin and floating the OSC<sub>2</sub> pin as shown in Figure 2. The master clock is used to derive the clock edges required by both the analog and digital sections. The device requires a 3.6864MHz master clock to derive the proper internal timing for Line Noise Rejection of either 50Hz or 60Hz.

The present revision of the production silicon operates as designed and meets all the documented specifications. We have discovered a possible degradation in the robust operation of the clock if care is not taken in the layout of your circuit, using a crystal between OSC<sub>1</sub> and OSC<sub>2</sub>. If care is not taken, the feedback (crystal) loop noise will result in a non reliable master clock, which in turn, will produce erroneous conversion results.

We have identified the cause and determined, if you use the following recommendation, you will not experience any degradation and the part will operate to the data sheet specifications. We have a design underway to improve the robust operation of the internal clock. We are also working on other enhancements that will be included in the next phase of the HI7188's evolution.

**Crystal Operation**

Using a crystal to generate the clock, care must be taken to minimize any external stray capacitance/inductance seen by the OSC<sub>1</sub> and OSC<sub>2</sub> pins. With the present version, we recommend the crystal be connected as close to the HI7188 device as physically possible. If you cannot meet these requirements, we would recommend you use an External CMOS Clock instead of the crystal.

**External CMOS Clock Operation**

When driving the HI7188 with an external CMOS clock, the clock should never be turned off. If the clock is turned off, the device should be re-synchronized by resetting either manually via the RESET pin or by the following special software instructions. The hardware reset will clear all registers and RAMs as defined in the data sheet. The software reset is achieved by either performing an I/O access of any calibration RAM or cycling the device through a sleep cycle.

**Calibration RAM Access**

To re-synchronize the conversion process the user may perform an I/O access of any calibration RAM (read or write). When the user performs this I/O access the microsequencer stops the conversion process, resets the modulator, digital filter and waits until the I/O is complete. After the I/O is completed the microsequencer automatically restarts the conversion process.

**Sleep Cycle**

Another method to re-synchronize the conversion process is to cycle the device through a sleep cycle. The user places the device in SLEEP mode by writing the SLP bit (CR<3>) of the Control Register to logic one. The microsequencer will stop the conversion process, reset the conversion pointer to logical channel one, clear the four line noise rejection filters and deactivate  $\overline{EOS}$ . The serial interface, calibration/data RAMs, CR and CCR are not affected.

To return from sleep mode the user changes the SLP bit from high to low. This restarts the conversion process beginning with logical channel 1. If line noise rejection (LNR) is enabled, it takes four complete scans (all eight channels) to refill the four line noise rejection filters before an  $\overline{EOS}$  interrupt. If LNR is not enabled, it takes one conversion scan of only the active channels before an  $\overline{EOS}$  interrupt. Recalibration is not required since the calibration RAMs are not effected by the sleep operation.

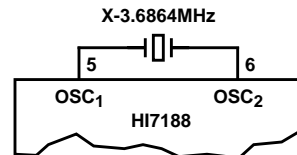


FIGURE 1. CRYSTAL OPERATION

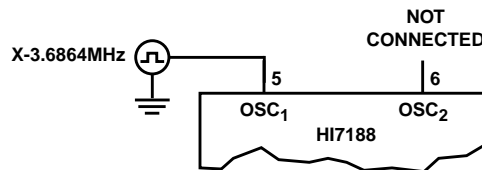


FIGURE 2. CRYSTAL OPERATION

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