

One of the design rule checks in DECIMATE™ is that the output rate must be greater than 2 times the sum of passband + transition band. For the informed user, violation of this rule is a valid design choice. Suppression of this rule check in DECIMATE is not possible, but design of such a filter using DECIMATE is possible.

The general solution is to use DECIMATE to design a filter with an output rate that is twice the desired rate, or a integer multiple of the desired rate that is >2(pass + trans). Outside of the Design Module the FIR decimation rate is increase by the factor needed to achieve the desired output rate. The new filter response is obtained graphically.

Consider a filter with a passband of 70kHz and a transition band of 60kHz. The desired output rate is 200kHz. DECIMATE requires an output rate of >260kHz, an output rate of 400kHz is chosen (see Figure 1 below and FILTER 1 page 2).

By increasing the FIR decimation by a factor of 2, the folding point ($f_s/2$) is moved and the desired output rate is obtained. The filter response can be generated graphically. The aliasing component is represented by the dotted line (see Figure 2 below).

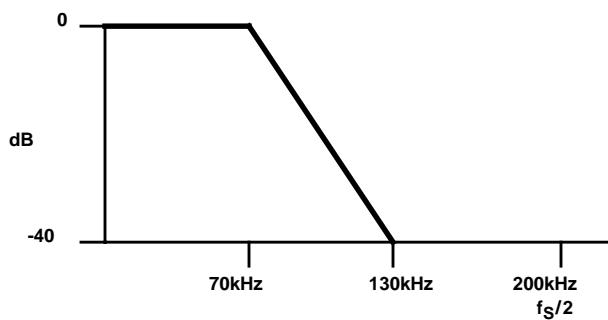


FIGURE 1.

Notice in FILTER 1 the stopband attenuation was limited to 40dB (FIR_CK=CK_IN). Because the FIR decimation was increased from 5 to 10, there are more taps available with FIR_CK=20MHz. Using Equation 2.0 from the 43220 Data Sheet, we see how many taps are available.

$$2\left(\frac{20(10)(10)}{20} - 10 - 4\right) = 172$$

We can therefore, use FILTER 2 which uses 151 taps and has 96dB stopband. The part will of course be programmed for FIR decimation rate of 10 and an FIR_CK of 20MHz is used.

To correctly simulate or generate PROM files for the “new filter” the *.DAR file must be edited. The corrected value for FDRATE on line 1, column 4 is entered. The correct output rate and FIR_CK rate are entered on the next to the last and the last line of the *.DAR file.

The above procedure works for standard or Precomp FIR. Remember the maximum3- FIR decimation rate is 16.

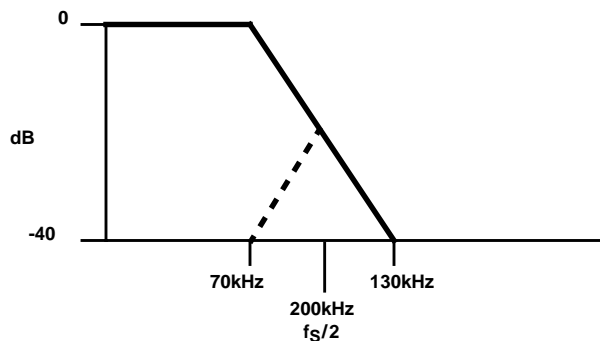


FIGURE 2.

DESIGN MODULE	SIMULATOR MODULE		PROM MODULE
HSP43220 DDF FILTER SPECIFICATION			
D E C I • M A T E	FILTER FILE	: filter1.DDF	
	INPUT SAMPLE RATE	: 20MHz	DESIGN MODE : AUTO
	OUTPUT RATE	: 400MHz	GENERATE REPORT : YES
	PASSBAND	: 70MHz	DISPLAY RESPONSE : LOG
	TRANSITION BAND	: 60MHz	SAVE FREQ RESPONSES : NO
	PASSBAND ATTEN	: 0.1dB	SAVE FIR RESPONSE : NO
	STOPBAND ATTEN	: 40dB	
	FIR TYPE	: STANDARD	
	HDF ORDER	: 2	FIR INPUT RATE : 2MHz
	HDF DECIMATION	: 10	FIR CLOCK (MIN) : 20MHz
	HDF SCALE FACTOR	: 0.78125	FIR ORDER : 81
			FIR DECIMATION : 5

FIGURE 3. FILTER DESIGN USING STANDARD TECHNIQUE

DESIGN MODULE	SIMULATOR MODULE		PROM MODULE
HSP43220 DDF FILTER SPECIFICATION			
D E C I • M A T E	FILTER FILE	: filter2.DDF	
	INPUT SAMPLE RATE	: 20MHz	DESIGN MODE : AUTO
	OUTPUT RATE	: 400MHz	GENERATE REPORT : YES
	PASSBAND	: 70MHz	DISPLAY RESPONSE : LOG
	TRANSITION BAND	: 60MHz	SAVE FREQ RESPONSES : NO
	PASSBAND ATTEN	: 0.1dB	SAVE FIR RESPONSE : NO
	STOPBAND ATTEN	: 96dB	
	FIR TYPE	: STANDARD	
	HDF ORDER	: 4	FIR INPUT RATE : 2MHz
	HDF DECIMATION	: 10	FIR CLOCK (MIN) : 40MHz
	HDF SCALE FACTOR	: 0.61035	FIR ORDER : 151
			FIR DECIMATION : 5

FIGURE 4. FILTER DESIGN DISREGARDING FIR CLOCK (MIN)

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