

Operation and Programming

Typical operation of the part using DECI•MATE software is as follows. $\overline{\text{RESET}}$ is held low long enough to satisfy the specification of 4 clocks for the slowest clock. Coming out of reset both start inputs must be high. After waiting the specified reset recovery time the registers are then loaded. H_Register1: H_DRATE Register will accept values from 0 to 1023. H_BYN is set as desired. F_CLA is typically set to a zero, F_DIS is set to a zero. H_Register2: H_STAGES is set as desired, a six or seven may be entered and will be interpreted as a five. H_GROWTH is entered as specified in the data sheet or DECI•MATE with acceptable values from 0 to 63, with values above 50, the most significant bits of the input data will be dropped. F_Register: F_TAPS will accept values from 2 to 511. DECI•MATE always generates odd tap filters, therefore, the value N to be entered will typically be even. F_DRATE, enter value between 0 and 15 as desired. F_ESYM, as with most filter design software, DECI•MATE always generates even symmetric filters, enter a one. F_BYN, enter as desired. F_OAD, typically set to a zero, used only for non-symmetric filters and for verifying filter coefficients. FC_Register, for the value N loaded in the F_TAPS Register there will be $(N/2)+1$ coefficients to be entered for odd length filters and $N/2$ coefficients for even length filters. It takes two writes to load each coefficient. Internally the number of coefficients loaded is recorded and used to determine the length of the filter, NOT F_TAPS. F_TAPS is used to offset a read pointer in the data RAM and to determine if an odd or even number of taps is being done to properly handle the center tap.

With programming of the HSP43220, the part must be started as described in the data sheet. If $\overline{\text{STARTIN}}$ is used, it will be the third rising edge of CK_IN (from $\overline{\text{STARTIN}}$ active) that the DATA_IN pins will start accepting data. If $\overline{\text{ASTARTIN}}$ is used it will be the fifth rising edge of CK_IN.

If at any time $\overline{\text{RESET}}$ goes active, or glitches low, the above procedure must be repeated (except for reloading coefficients). Also see reprogramming.

Implementing Non-symmetric Filters

The HSP43220 can implement up to a 256 tap non-symmetric filter. Correct programming procedures are as follows: By definition the number of coefficients loaded is equal to the number of taps (N). The F_TAPS is set equal to $2N-1$, and F_OAD and F_SYM are set to a one. The remaining registers are loaded normally.

Data in Bus

In many cases the source of information to be fed into the DATA_IN pins will be less than 16 bits wide. The recommended configuration is to connect the input bus to the most significant bits of DATA_IN and to tie unused DATA_IN pins to GND. In some systems there will be available a 16 bit bus to connect to the DATA_IN pins, but the full range of the bus is not being used. For example the upper 4 bits are always sign bits. This can be adjusted for in software by setting the growth for three more than normal. Even if the HDF is to be bypassed this can be accomplished by manually putting the HDF in bypass. This is done by setting H_STAGES and H_DRATE to 0. For the case described above, H_GROWTH would be set to $50+3$, or 53. This pushes the 3 extra sign bits off the top of the data shifter.

Output Format

As stated on page 4-5 of the DECI•MATE Manual, the FIR coefficients are computed using the Parks-McClellan (Remez) method and then scaled by the inverse of the HDF scale factor as well as an additional factor which accounts for the maximal ripple gain of the derived FIR. As a result, the output format is as follows: DATA_OUT bits 0-15 are the most significant bits. If OUT_SELH is held high, then DATA_OUT bits 16-23 are simply sign extension, if held low they are the LSB extension, for a total of 24 bits of resolution. For those that wish more bits of resolution the sign extension bits can be used. This may be accomplished through the users own software or the coefficients from DECI•MATE may be scaled. This is accomplished by determining the magnitude of the largest coefficient, and then multiplying all coefficients by the factor $0.999999/\text{mag}$. The coefficients must then be quantized to 20 bits. This results in the magnitude of the largest coefficient being about 0.999999, the largest representable value. This procedure also allows the realization of filters of greater than 96dB attenuation since it reduces quantization effects. The new position of the decimal point in the output will be moved into the sign extension bits with its exact position being dependent on the coefficients.

Bypass Modes Of The HDF And FIR

When the H_BYN bit is set, H_Register2 bits are affected as follows: H_GROWTH is set to 50, H_STAGES is set to zero. The clock divider is disabled so $\text{CK_DEC}=\text{CK_IN}$. The H_Register1 value H_DRATE is not altered by setting the H_BYN bit. H_Register2 must be reloaded after H_BYN has been returned to a zero.

With H_BYP set to a one, the feedback paths in the integrators and the holding registers in the comb are zeroed. The 16 bits of chip input data pass through the HDF section unaltered. As always, the first data sample out of the HDF (after reset/startup) is a zero due to resetting of the data paths. Because the FIR Section has several operations to complete between rising edges of CK_DEC, it is necessary for FIR_CK to be faster than CK_IN as described in the data sheet. The duty cycle of CK_IN must meet the conditions described in Tech Brief TB312. DECIMATE can be used to determine the necessary frequency of FIR_CK or Equation 1.0 in the data sheet can be solved for the case of HDF in bypass by setting Hdec=1.

When the F_BYP bit is set the FIR filter is configured as a 3 tap, even symmetric filter, no decimation with one input to the pre-adder set to zero (same side as if F_OAD was set). The output of the coefficient ram is forced to 00004H to aid in positioning the result in the accumulator. The output multiplexes are set by the F_BYP bit to output data from the bottom of the accumulator. For a 3 tap filter there are two multiply/accumulate (MAC) cycles. The data flow is as follows: A new piece of data becomes available at the HDF output as signaled by a rising edge of CK_DEC. The FIR is signaled and the data is written into the data ram. The first MAC cycle begins. From the data ram the new data and some old data are read. The new data is added to zero in the pre-adder, then multiplied by the coefficient, and then accumulated with a zero (because start of new FIR cycle). The second MAC cycle starts one FIR_CK cycle after the first. Two old pieces of data are read from ram. But two zeros are input to the pre-adder because of zeroing the other side of the pre-adder at the center of odd length tap filters. The resulting zero is multiplied by the coefficient and accumulated. The accumulator results are sent to the output pins along with a DATA_RDY.

Reprogramming

After initial startup of the HSP43220 the FIR Section can be reprogrammed using the F_DIS bit of H_Register1. When writing H_Register1, be sure to maintain the same values in bits 0-10, H_DRATE and H_BYP. When the F_DIS bit is written the FIR Section will terminate a FIR cycle if one is in progress, no DATA_RDY is issued. The FIR Section is disabled from performing multiply/accumulate cycles. The FIR_CK must continue to run. The HDF Section continues to operate and its output continues to be written into the data ram. By letting the HDF Section continue to run, the synchronous operation of multiple DDFs is maintained. By continuing to load the data ram a transient response is avoided when the FIR Section is restarted. Writing the F_DIS bit also resets the coefficient ram address pointer to zero (to allow for reloading coefficients) and enables writing of the coefficient ram (writing is disabled when FIR Section is enabled). Once the bit is set and at least two rising edges of FIR_CK have occurred, the user may then reconfigure the

FIR Section as desired. The FIR Section can be re-enabled either by writing F_DIS to a zero or by generating a high to low transition on either of the start inputs, which automatically clears F_DIS.

For those users that wish to clear the HDF data paths before bringing in a new signal, or for those that wish to change HDF programming and have multiple DDFs running synchronously, activating the $\overline{\text{RESET}}$ input is recommended. Re-programming the DDF and restarting will be necessary. The coefficient ram is not corrupted by reset and will not need to be reloaded unless new coefficients are needed. It is also possible to reconfigure the HDF without losing synchronization between DDFs if CK_IN is stopped (high or low) during writing of the registers. For single chip applications or where synchronization is not a concern, the HDF Registers can be written on the fly. This will result in a transient response and changing HDF Registers at regular intervals in an attempt to achieve fractional decimation rates with the chip is not recommended.

Internal Decimation

The total decimation in the DDF, also called the system decimation, is equal to the product of Hdec and Fdec. The output rate of the DDF will be equal to CK_IN divided by system decimation, regardless of FIR_CK speed. The time from the start of the DDF to the first DATA_RDY may not be the same as time between DATA_RDYs. To the user the FIR decimation appears at the FIR output. That means the output of the DDF is equivalent to using a standard FIR filter and only looking at every Nth output for FIR decimation of N.

In the HDF the counter used for decimation is initialized to Hdec. The first CK_DEC (internal to chip) will occur about Hdec CK_INs after the part is started. The FIR decimation counter is initialized to zero and the first CK_DEC will always cause a FIR cycle which generates a DATA_RDY about taps/2 FIR_CKs later. Thus, the time delay from start of the DDF to the first DATA_RDY is about CK_IN period times Hdec plus, FIR_CK period times taps/2.

Transient Response

After reset, after changing the source of input data, or after re-programming the HDF, the output of the DDF will have a transient response until the data ram is sufficiently full of "valid" data. There is no transient response when only the FIR is reprogrammed using the FIR disable bit in the control register. It is impossible to predict exactly when the transient is complete, as the answer depends on the FIR filter coefficients as well as new data values relative to old data values in both the FIR and HDF.

First the integrator stage(s) must be flushed of old data (except when reset is used). The number of stages and growth will influence this. But in general the flushing of the integrator stages is small compared to the remainder of the chip. For N stages it will take N CK_DEC cycles to flush all

the holding registers in the comb. The number of taps determines how many locations of the data ram needs to be written with new data. The equation for the number of input samples needed to complete the transient response is:

$$\text{number of input samples} = H_{\text{dec}}(\text{taps} + N)$$

The number of output samples that are part of the transient response is:

$$\text{number of output samples} = \text{taps}/F_{\text{dec}} + N/F_{\text{dec}}$$

Because the center coefficients are usually much larger than outer coefficients the transient response is done before all the ram locations are filled. In some cases in half the time described above.

The simulator in DECI•MATE assumes all unwritten ram locations are zero and may not necessarily reflect the startup transient of the DDF. This can be overcome by making sure leading zeros are input ahead of the signal for both the simulator and the chip. For the case of the data input changing (one signal followed by another) the simulator will match the DDFs transient response. You cannot simulate reprogramming the DDF.

Clock Inputs

The requirement that the two input clocks be synchronous is driven by the handshake circuitry between the HDF and FIR Section. In this circuitry there is a flip/flop which has CK_DEC as the data input and FIR_CK as the clock input. Based on the theory that it is impossible to design a synchronizer that is 100% immune to metastable conditions, it was needed to specify the FIR_CK and CK_IN inputs as synchronous inputs. Metastable condition refers to when the flop output oscillates due to the data and clock changing simultaneously. For the user that finds it very inconvenient to use synchronous clocks, or for one that does not wish to use clocks that are integer multiples (which is by definition not synchronous), the use of a local synchronizer can be of benefit. This option puts the risks and control of metastability at the board level under user control. One example of this might be a user that has designed the needed filter in DECI•MATE and the required FIR_CK is 35Mhz with a CK_IN rate of 5Mhz. Through the use of Equation 1.0 in the data sheet, the minimum FIR_CK is 32Mhz. The software chose 35Mhz because it is the smallest integer multiple (30Mhz would have been too slow). Assume the fastest available speed grade of HSP43220 is 33Mhz. The user may then use a local synchronizer to make the filter realizable. The following is just one example of a local synchronizer that re-aligns the system clock edges to create a synchronous CK_IN.

The following restrictions are needed to ensure maximum performance:

1. System clock must have high and low times greater than oscillator period.
2. Have to still meet DATA_IN setup and hold times at DDF pins. Use of Q bar output makes this easier.
3. Realistically the maximum system clock rate is one sixth of oscillator.

Node A can still become metastable but it has one oscillator period to become stable. The user has access to node A and can make his own evaluation as to if the circuit performance is acceptable. In general, the higher the speed capabilities of the flip/flops used makes for faster resolution of the metastable condition if it should occur.

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