



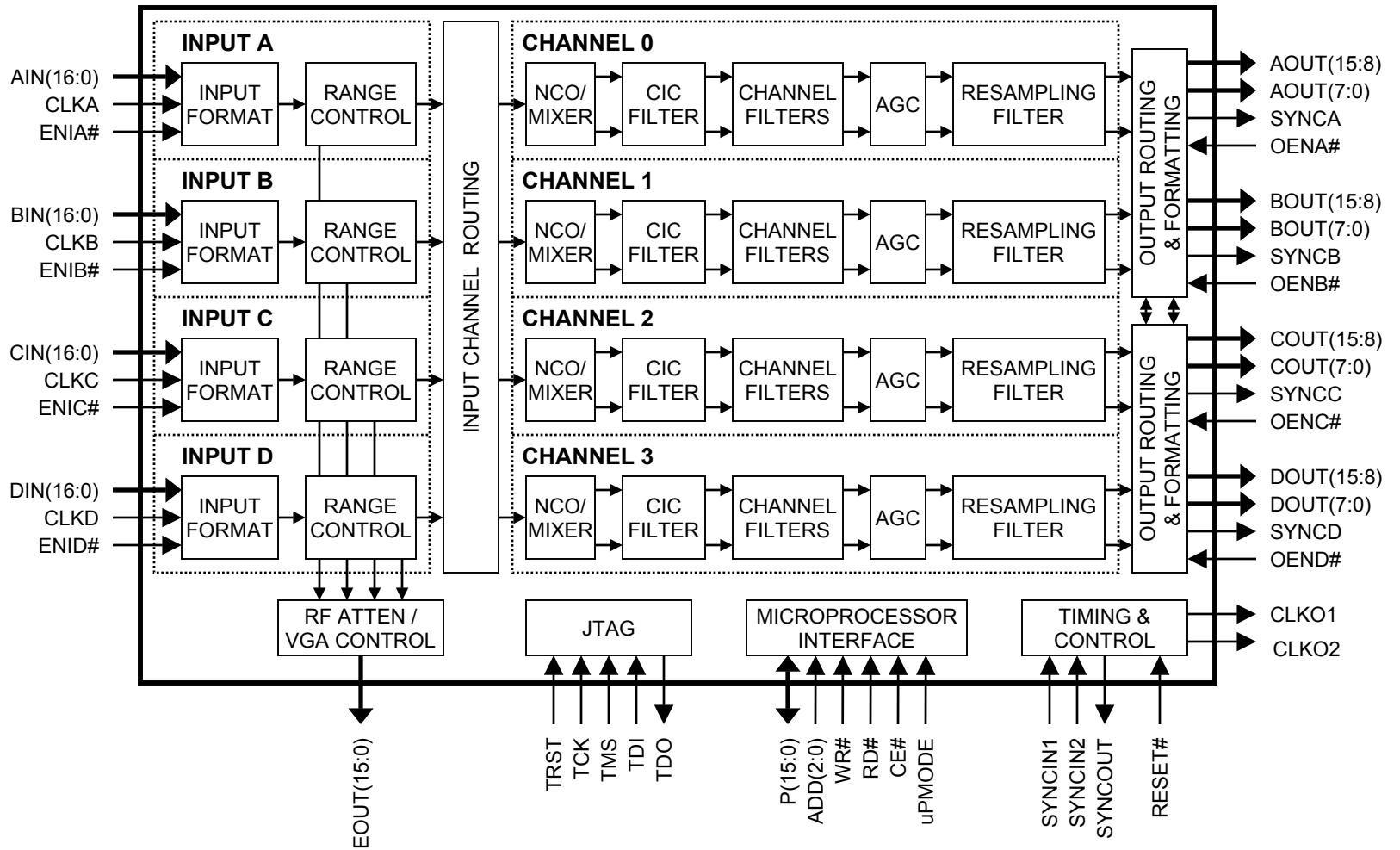
ISL5416
Quad Wideband
Digital
Downconverter



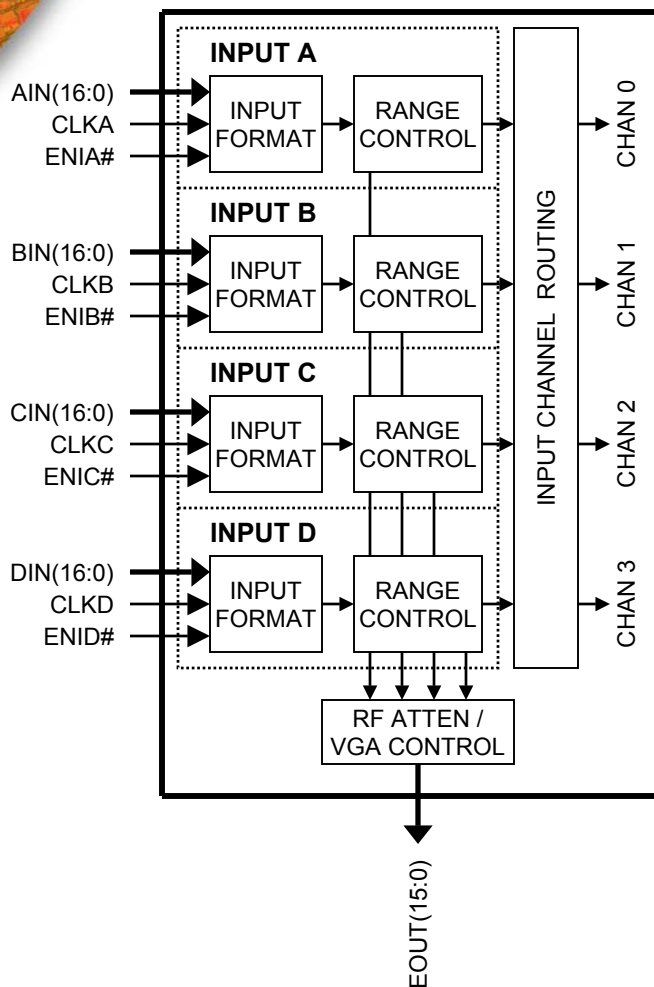
ISL5416 Quad 3G Down Converter

- **Features:**
 - **Quad Wideband Programmable Down Converter**
 - **Four independent channels**
 - **95MSPS max input sample rate**
 - **Four input buses, each with A/D range control**
 - **5MHz BW/channel with full filtering**
 - **Higher BW/channel supported with reduced filtering**
 - **Higher effective BW via multi-channel polyphasing or cascading**
 - **AGC with 96 dB Range**
 - **Interpolation and Resampling Filters**
 - **Parallel, Serial, and Sequenced uP Read Outputs Modes**
 - **16-bit indirect control interface similar to ISL5216**
- **Technology:**
 - **Fabricated in 0.18u CMOS with 3.3V I/O pads**
 - **17 x 17mm 256CABGA (1.0mm) package**

ISL5416 Block Diagram

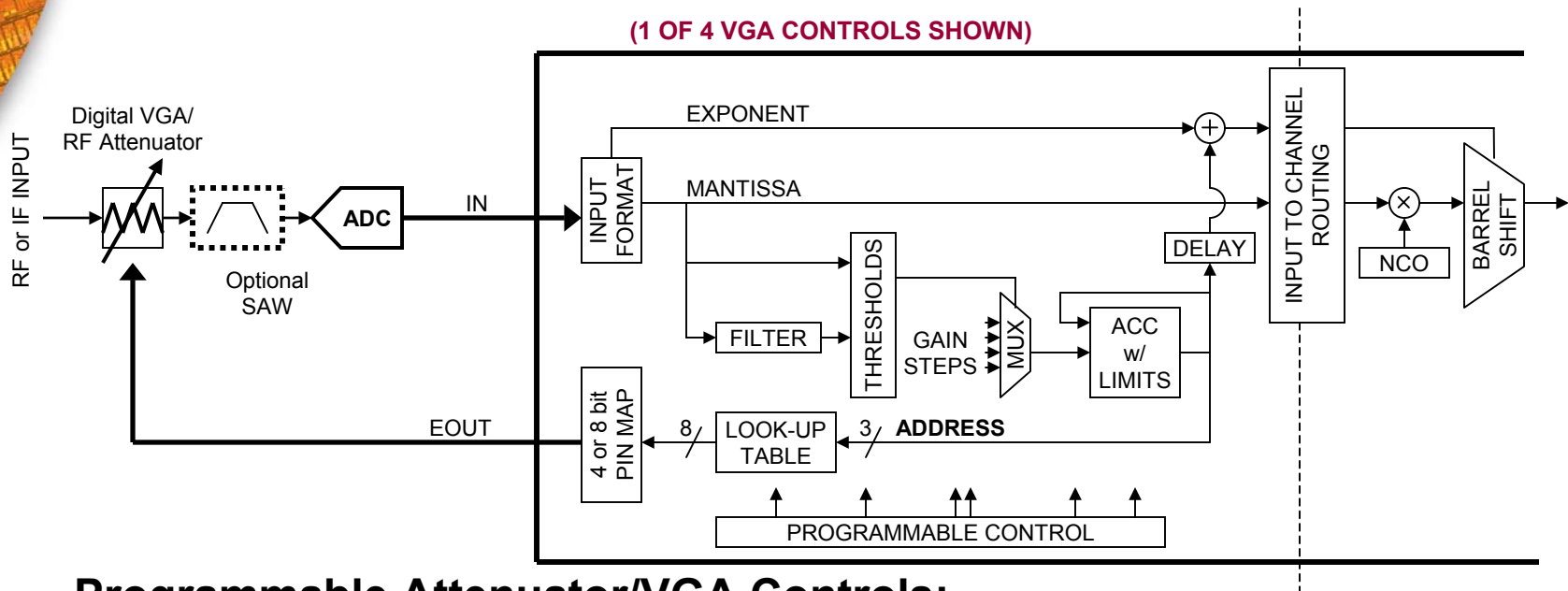


ISL5416 Input Features



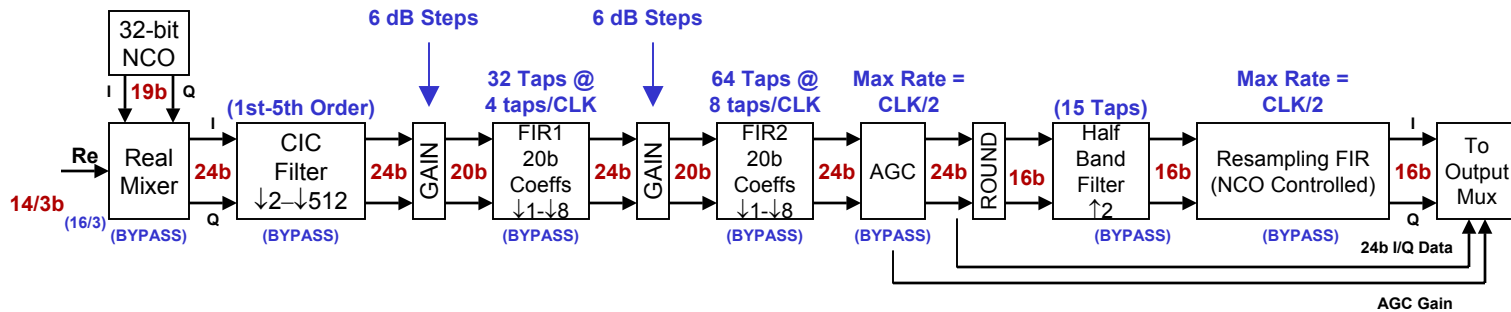
- **Max Input Sample Rate = 95 MSPS**
- **Separate input clocks to allow for timing skew between multiple ADC's**
 - Inputs re-sync'd to master clock (CLKC)
- **Input Formats supported per input bus**
 - 16 bit Fixed Point OB or 2's Comp Binary
 - 17 bit Floating Point Real (14M/3E)
- **ADC Input Range Control for each channel via shared/partitioned 16-bit RF Attenuator / VGA Control bus**
- **Input Channel Routing**
 - Switches any input bus to any down converter channel

ISL5416 Range Control



- **Programmable Attenuator/VGA Controls:**
 - Time Slot Interval and Delay and from SYNCINx
 - 0 - 42 dB of Attenuator/VGA Control Range
 - Comparator thresholds and hold-off
 - Look Up Table (LUT) mapping Gain -> Atten/VGA interface control
 - Exponent delayed sum to match system group delay
- **Example External Devices:**
 - M/A-COM AT90-1263 RF Attenuator
 - National CLC5526 Digital VGA (0-350MHz)

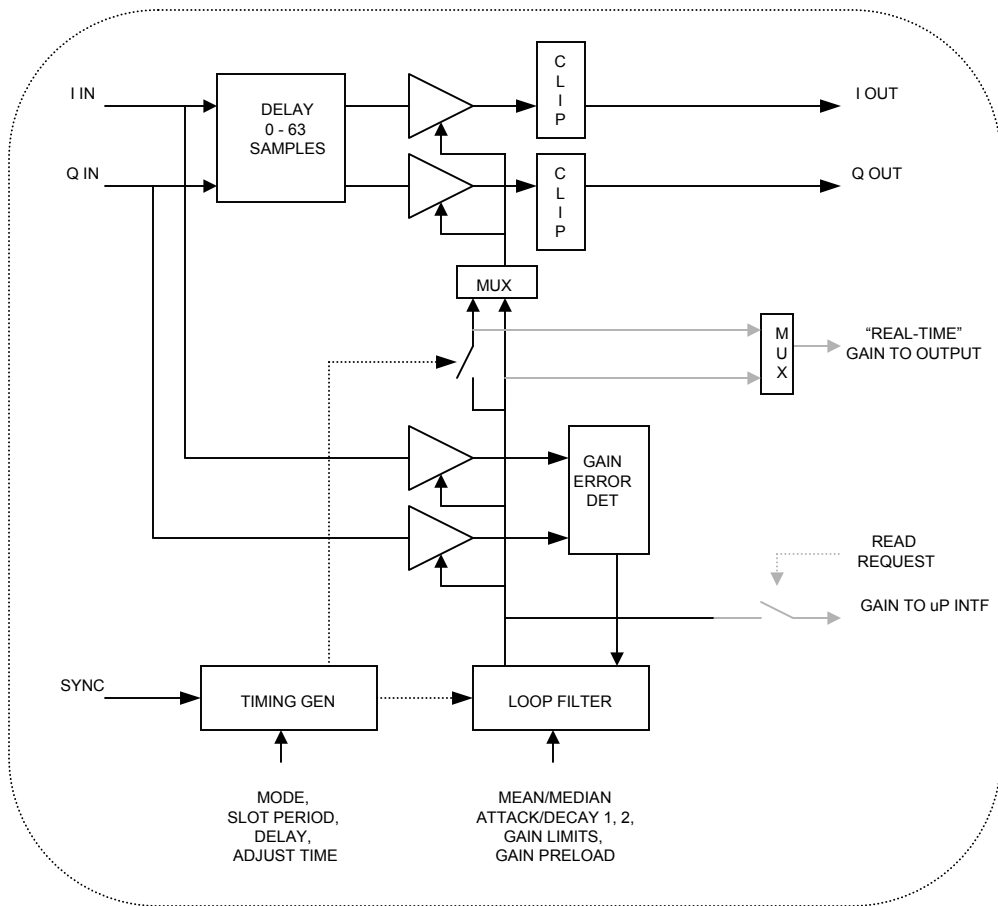
ISL5416 Channel Architecture



Channel Features

- 95 MSPS Input Sample Rate
- Fully programmable FIR filters
- 5MHz channel BW with full filtering
 - 10MHz BW with reduced filtering
- >110db SFDR and OOB Attenuation
- 96dB AGC Range
- Resampling Filter for Non-Integer Sampling Rates

ISL5416 Channel AGC



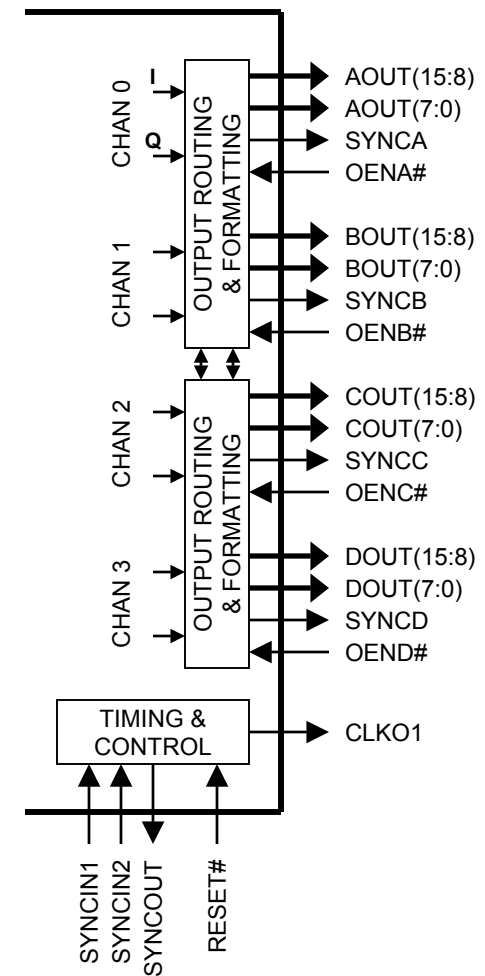
ISL5416 CONCEPTUAL AGC BLOCK DIAGRAM

The “real-time” gain is provided to the parallel output, serial output, and sequenced read uP outputs. The sampled or requested read gain is only available at the sequenced read on the uP interface.

Note that the “real-time” gain can be either the gain from the loop filter or the sampled gain from the loop filter. Though the sampled gain was intended for the sampled AGC mode, it will update in the timed mode when the duration counter reaches zero. This update can be aligned to the time slots, allowing the AGC gain to be sampled and held at the same time each slot whether or not the sampled AGC mode is used. (Production silicon only)

ISL5416 Output Features

- Eight 8 bit parallel output busses supporting:
 - 4, 6, 8, 12, 16, 20 or 24 bit data formats
 - Example bus configurations:
 - 8 x 8 bit
 - 4 x 16 bit
 - 2 x 32 bit
 - Separate or Mux'ed I/Q data output
 - Up to 16 bit AGC gain data outputs available
- All data synchronized to single CLKO
- Multiplexed channels supported if channels are synchronized:
 - Up to 8 timeslots/frame
 - Frames synchronized to SYNCx outputs
- Serial Outputs available on DOUT
- Sequenced uP Read Ports



ISL5416 Output Routing Example (4 channels routed to single output bus)

UMTS Example:

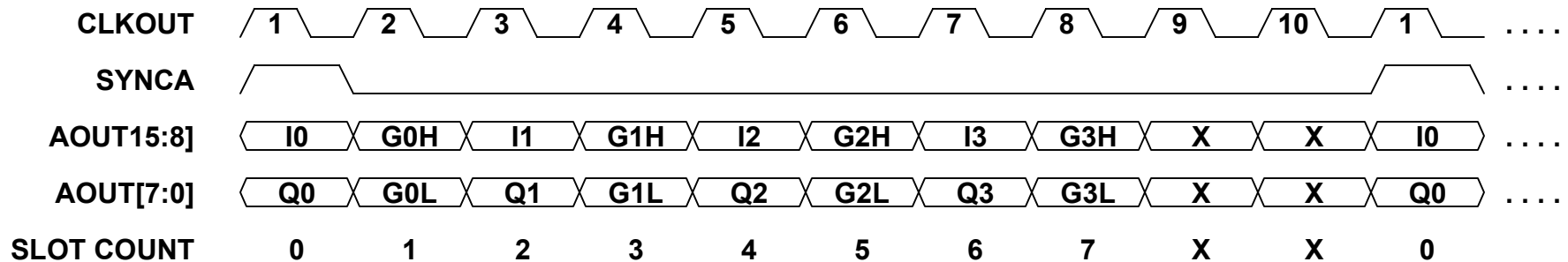
Input Sample Rate (CLKA) = 76.8MSPS (20x oversample of 3.84Mcps)

Output Data Rate = 7.68MSPS (2x oversample rate)

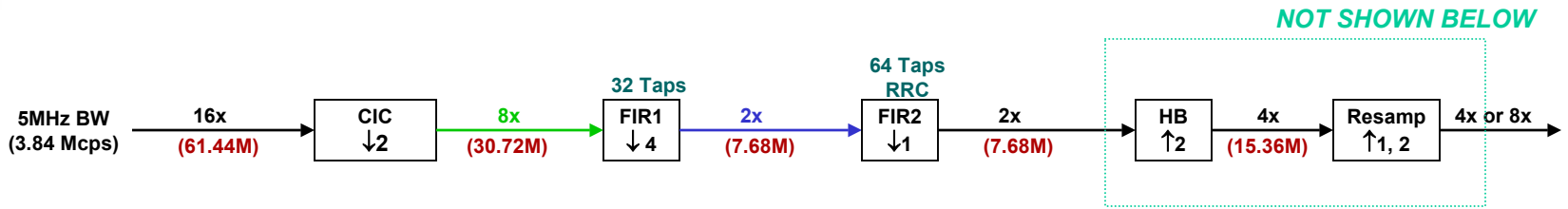
Thus, 20x/2x = 10 CLKOUT cycles per frame

Configuration: Multiplex 4 channels of 8-bit I/Q and 16-bit AGC data on single AOUT bus

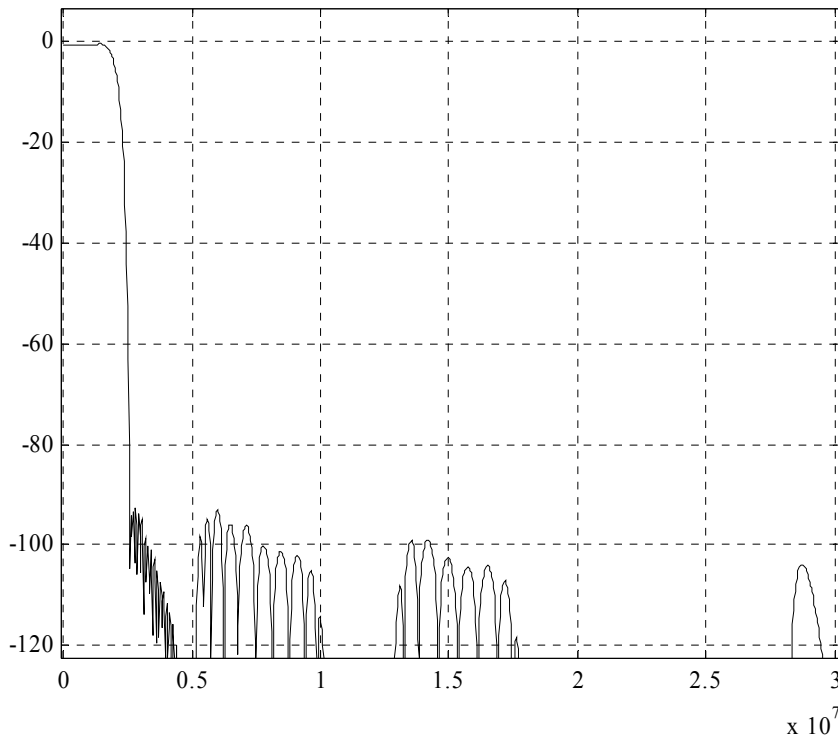
CLKOUT Cycle	Slot Count	SYNCA	AOUT[15:0]	Description
1	0	1	Q0[7:0],I0[7:0]	Channel 0 8-bit I/Q data
2	1	0	G0[15:0]	Channel 0 16-bit AGC data
3	2	0	Q1[7:0],I0[7:0]	Channel 1 8-bit I/Q data
4	3	0	G1[15:0]	Channel 1 16-bit AGC data
5	4	0	Q2[7:0],I0[7:0]	Channel 2 8-bit I/Q data
6	5	0	G2[15:0]	Channel 2 16-bit AGC data
7	6	0	Q3[7:0],I0[7:0]	Channel 3 8-bit I/Q data
8	7	0	G3[15:0]	Channel 3 16-bit AGC data
9	X	X	X	idle
10	X	X	X	idle



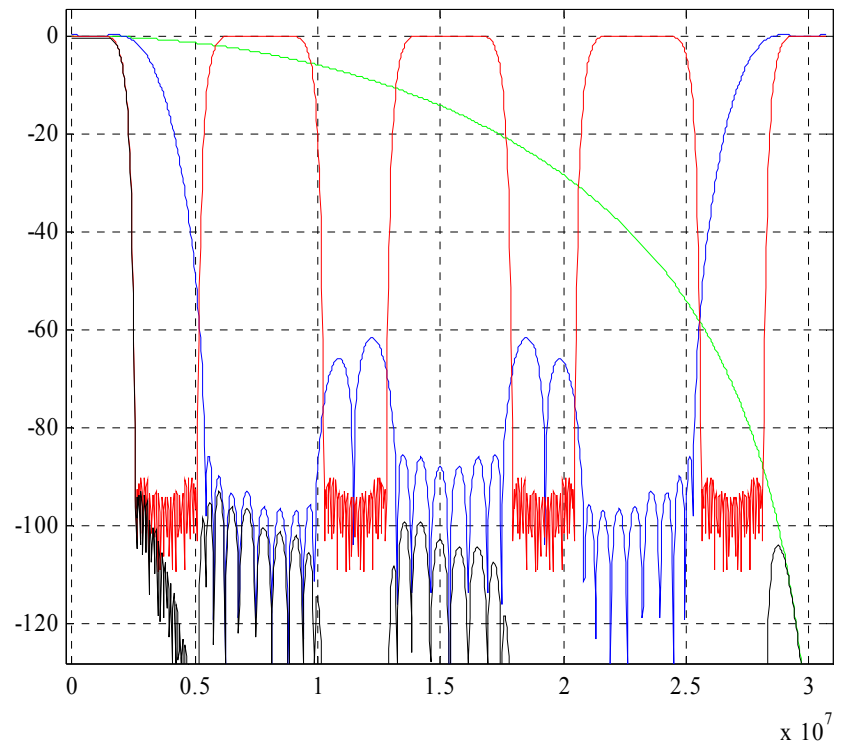
ISL5416 Composite Response WCDMA Example



Composite Response (Zoom Out) 0-30MHz



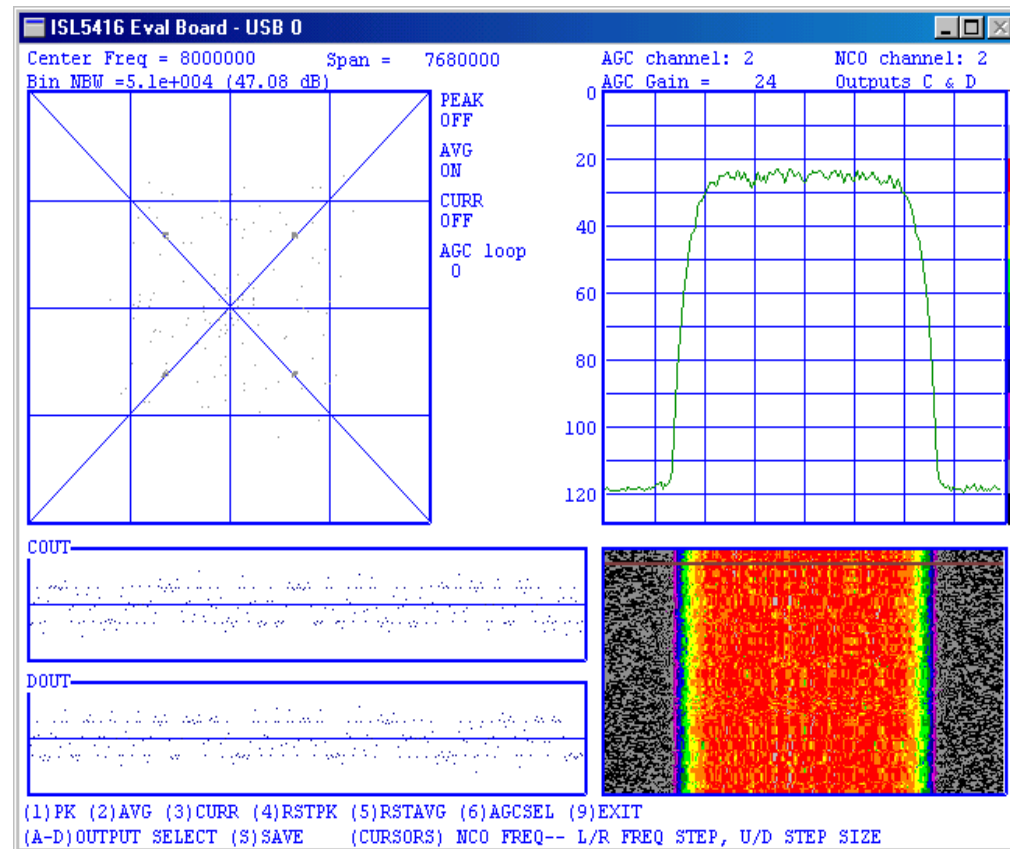
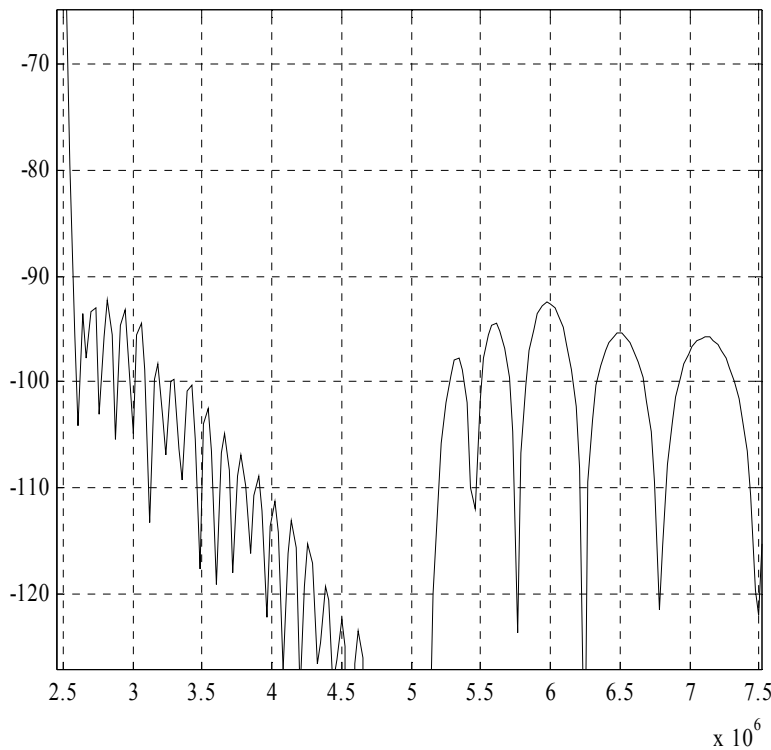
Filter Response Overlay (Green = CIC; Blue = FIR1; Red = FIR2; Black = Composite)



ISL5416 Composite Response WCDMA Example

2x Chip Rate Output, 16 bits

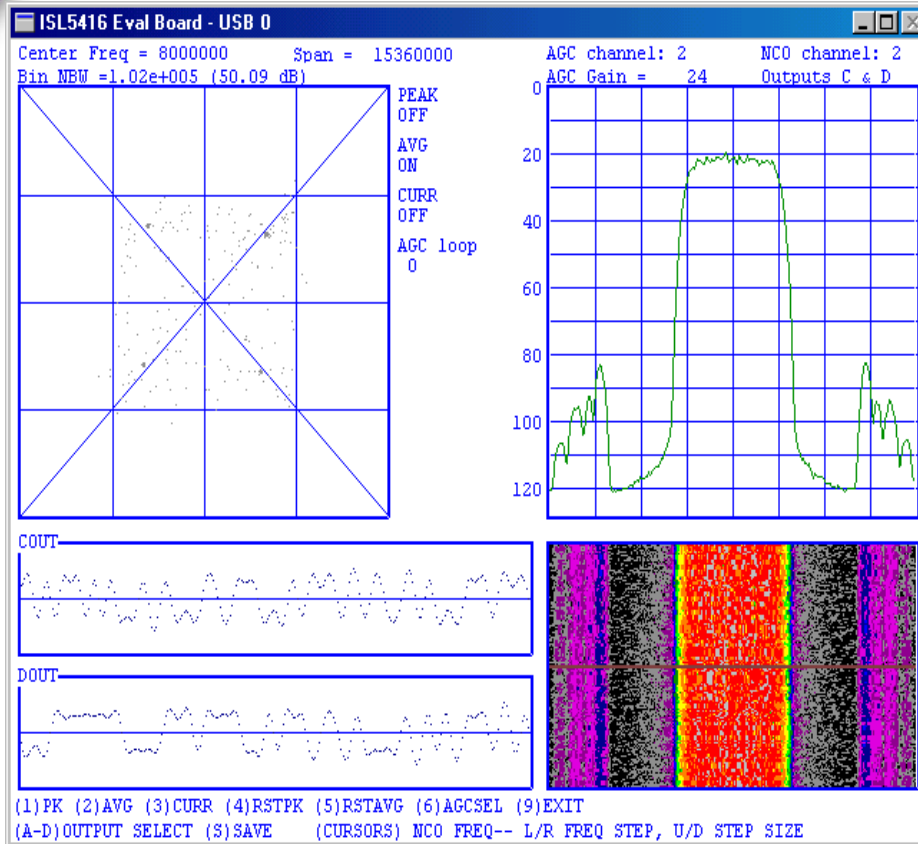
Adjacent Channel Rejection



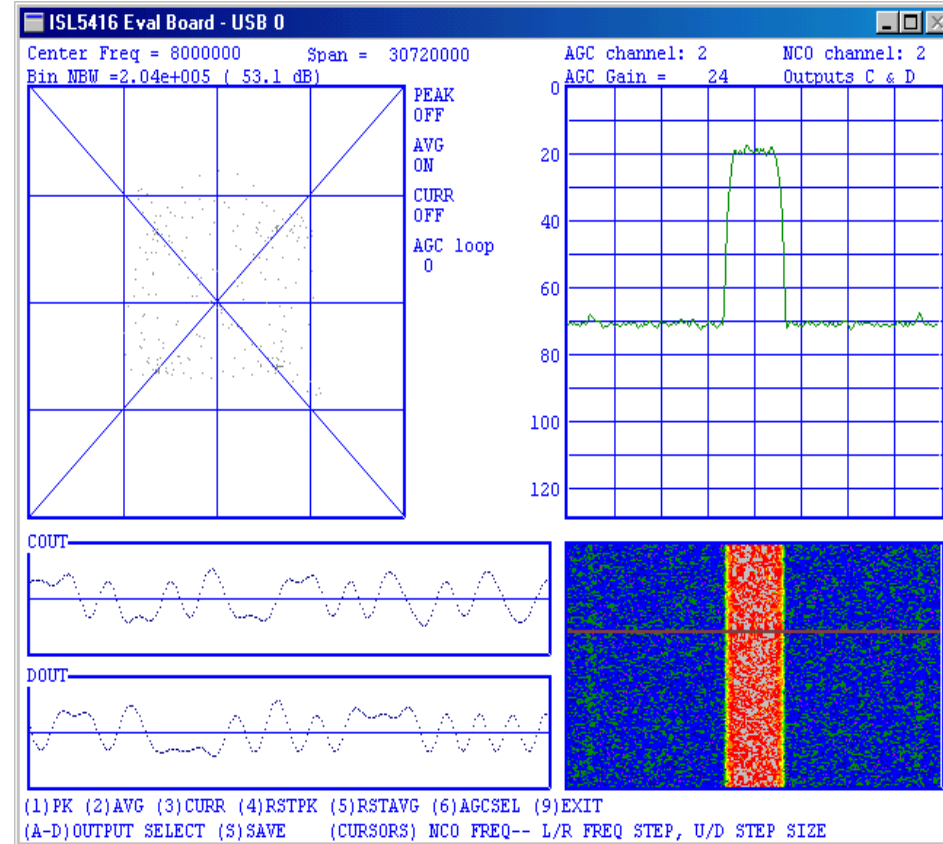
ISL5416 Composite Response WCDMA Example

4x Chip Rate Output, 16 bits (showing interpolation images)

8x Chip Rate Output (30.72 Msps), 8 bits



IHBF Enabled



IHBF and Resampling Filter