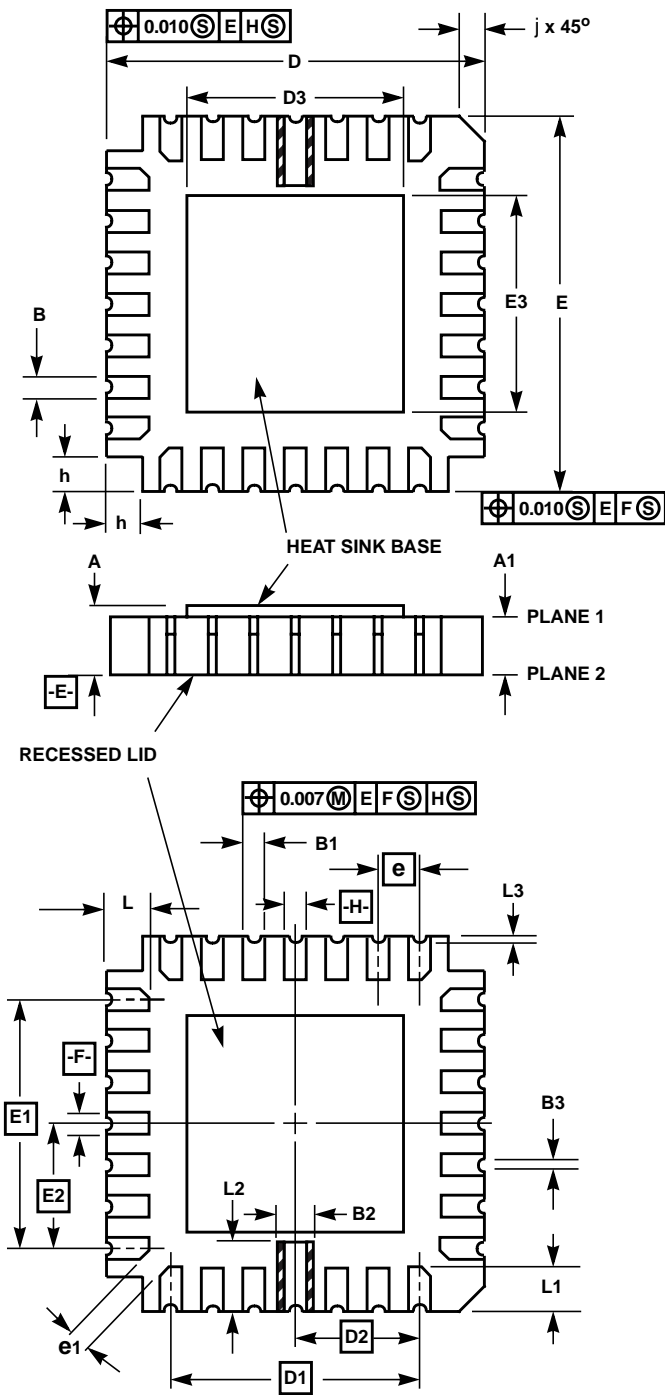


Ceramic Leadless Chip Carrier Packages (CLCC)



J68.B
68 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.118	2.34	3.00	6, 7
A1	0.067	0.083	1.71	2.11	-
B	0.033	0.039	0.83	0.99	-
B1	0.033	0.039	0.83	0.99	2, 4
B2	0.072 Ref		1.83 Ref		-
B3	0.006	0.022	0.15	0.56	-
D	0.940	0.960	23.88	24.38	-
D1	0.800 BSC		20.32 BSC		-
D2	0.400 BSC		10.16 BSC		-
D3	0.695	0.705	17.65	17.91	2
E	0.940	0.960	23.88	24.38	-
E1	0.800 BSC		20.32 BSC		-
E2	0.400 BSC		10.16 BSC		-
E3	0.695	0.705	17.65	17.91	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.050 Ref		1.27 Ref		5
j	0.020 Ref		0.51 Ref		5
L	0.042	0.058	1.07	1.47	-
L1	0.042	0.058	1.07	1.47	-
L2	0.080	0.090	2.03	2.29	-
L3	0.003	0.015	0.08	0.38	-
ND	17		17		3
NE	17		17		3
N	68		68		3

Rev. 1 5/28/97

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across all of the ceramic layers to make electrical connection with the required plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and required plane 2 terminals shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.