

**Radiation Hardened Power-Up/Down
Microprocessor Reset Circuit**



The Radiation Hardened IS-705RH is a monolithic device that monitors the power supply voltage used by satellite control units and provides a

reset output pulse during power-up and power-down. The reset threshold is 4.65V (Typ) and the reset pulse width is set at 200ms (Typ). A watchdog circuit is incorporated for easy interfacing with microprocessors and controllers. If the watchdog input has not been toggled within a preset 1.6s (Typ) time period, an output signal is generated, which can be used as an interrupt. The power function input (PFI) may be used to monitor other voltage levels. The circuit has a 1.25V (Typ) threshold and provides a PFO output when low voltage is detected. An active-low manual reset input is also provided for direct control of the reset function.

Constructed with the Intersil UHF2X-CMOS process, these devices have been specifically designed to provide highly reliable performance in harsh radiation environments. This process has been tested for single event latch-up and has demonstrated an immunity to 90MeV/mg/cm².

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-00538. A “hot-link” is provided on our homepage for downloading.
<http://www.dscclia.mil/downloads/milspec/smd/00538.pdf>

Features

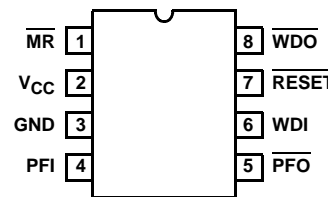
- Electrically Screened to SMD #5962-00538
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Hardness
 - Total Dose 100 krad(Si) (Max)
 - Single Event Latch-up >90MeV/mg/cm²
- Precision 4.65V Voltage Monitor
- Supply Voltage Range 4.75V to 5.5V
- $\overline{\text{RESET}}$ Valid at $V_{CC} = 1.2V$
- Low Supply Current 420 μ A (Typ)
- 200ms (Typ) $\overline{\text{RESET}}$ Pulse Width
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Flight Computers
- Controllers
- Critical Microprocessor Power Monitoring
- Reliable Replacement of Discrete Solutions

Pinout

**IS-705RH
(8 LD FLATPACK)
TOP VIEW**



Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
5962R0053801QXC	IS9-705RH-8	Q 5962R00 53801QXC	-55 to +125	8 Ld Flatpack, Solder SL	K8.A
5962R0053801VXC	IS9-705RH-Q	Q 5962R00 53801VXC	-55 to +125	8 Ld Flatpack, Solder SL	K8.A
5962R0053801V9A	IS0-705RH-Q		-55 to +125	8 Ld Flatpack, Solder SL	K8.A
IS9-705RH/Proto	IS9- 705RH /Proto	IS9- 705RH /Proto	-55 to +125	8 Ld Flatpack, Solder SL	K8.A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Die Characteristics

DIE DIMENSIONS:

1500 μ m x 1830 μ m (59mils x 72mils)
 Thickness: 483 μ m \pm 25.4 μ m (19mils \pm 1mil)

INTERFACE MATERIALS

Glassivation

Type: Nitride (Si₃N₄) over Silox (SiO₂)
 Nitride Thickness: 4.0k Å \pm 1.0k Å
 Silox Thickness: 12.0k Å \pm 4.0k Å

Top Metallization

Top Metal 3: TiAlCu
 Thickness: 0.8 μ m \pm 0.02 μ m
 Metal 1 and 2: TiAlCu
 Thickness: 0.4 μ m \pm 0.01 μ m

Metallization Mask Layout

Substrate:

UHF2X-CMOS

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION

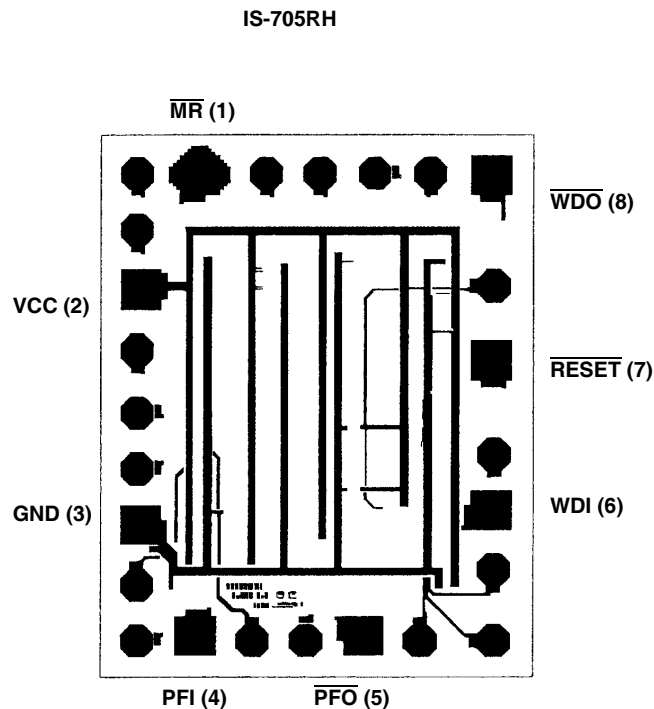
Substrate Potential:

Backside internally connected to GND
 (May be left floating or connected to GND.)

ADDITIONAL INFORMATION

Worst Case Current Density:

$<2.0 \times 10^5$ A/cm²



NOTES:

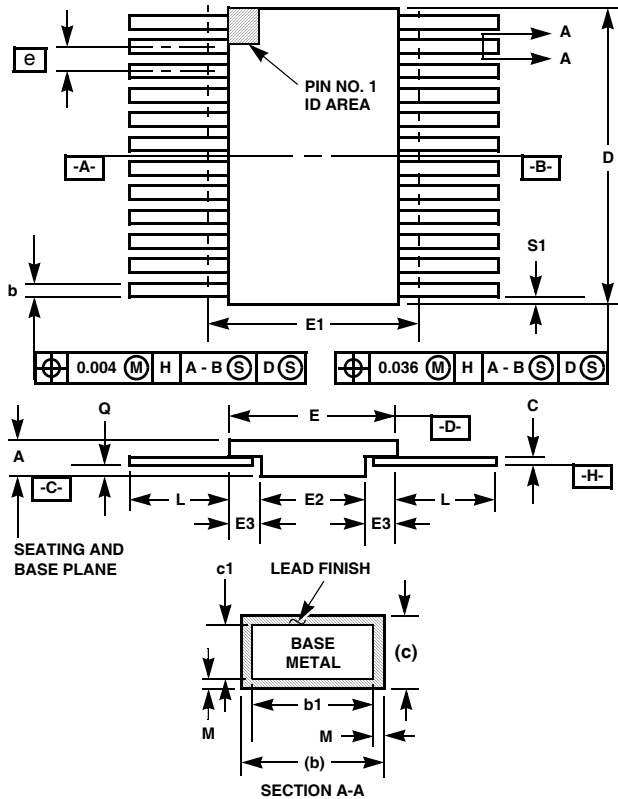
1. Octagonal trim pads should be left unconnected.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
 Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

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Ceramic Metal Seal Flatpack Packages (Flatpack)



K8.A
8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.070	0.115	1.18	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.007	0.10	0.18	-
D	0.245	0.265	6.22	6.73	3
E	0.245	0.265	6.22	6.73	-
E1	-	0.280	-	7.11	3
E2	0.170	0.180	4.32	4.57	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	-	-	-	-	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	-	0.66	-	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	8		8		-

Rev. 0 9/00

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.