iSIM ACTIVE FILTER DESIGNER

TECHNICAL DETAILS ON MULTI-STAGE SEQUENCING AND SALLEN KEY RC SOLUTIONS

Michael Steffes
Sr. Applications Manager
12/6/2010
Introduction to the New Active Filter Designer

This is presenting a new online design tool Intersil developed over 2009. This is a free tool along with the op amp macromodels and a very capable Spice simulator all available free in the Intersil web site.

- Scope and Intent
- Multi-stage gain partitioning and Q sequencing issues.
- 2nd Order Low Pass Stage Design (SKF and MFB)
- Discrete element implementation issues
- Some sensitivity issues and misconceptions corrected
- Design flow in the tool
Online Design Tool Issues and Constraints

Ideally, would like to take a target filter shape and deliver a set of op amps and external passives that accurately achieve the desired filter response.

Vendor tools need to have both strong design algorithms and the available implementation op amps in the tool and well modeled.

- Most vendor online tools design with ideal op amps – which is considerably easier to get design algorithms, but less useful to reach a production ready designs.
- Classic literature on SKF (Sallen Key) and MFB (Multiple FeedBack) 2nd order stages were simplified or working with the assumption that the op amps were slow and poorly controlled and the R’s and C’s had large tolerances and tempco’s.
- Both the op amps and passives have improved a lot and we should be able to take advantage of that to deliver successful designs that improve on dynamic range with a tight production tolerance.
- Pretty much all legacy active filter articles showing Monte Carlo spreads have been dominated by the 5 or 10% C tolerances. Low cost 1% C’s are available now and tighten these spreads considerably.
Typical Design Biases in Existing Vendor Tools

Gain of 1 is preferred for as many stages as possible

• This helps the sensitivity to Q vs. K issue for the SKF (for instance, with K=1 and $R_1 = R_2$, $\frac{S_{x}^{2}}{K} = 2Q^2$). But for the SKF with target Q >1.5, the gain of 1 design point has significant noise peaking internal to the stage. Increasing this to a gain of just 1.2 can reduce the noise gain peaking by >10dB with minimal sensitivity impact.

Equal R is preferred in the 2\textsuperscript{nd} order SKF low pass design

• This again comes from simplified sensitivity analysis. The more detailed analysis done to develop this tool proved that $R_1/R_2 < 1$ always moves in the direction of reduced noise gain peaking and better overall filter sensitivities.

Equal C is preferred.

• This is for designs headed to integration – this is not a constraint that really matters for board level design tool. There are constraints on the range of C values that are readily available, but holding them in close ratiometric match (or equal) can sometimes push the designs in directions that cost you in other areas.
Delivered C values from existing vendor tools.

Some tools fix one of the C’s to a constant value, then take what it needs for the others.
  - This artificially constrains the other C value.

Some allow the C’s to get very large in low frequency designs and/or do not snap to standard E24 values.
  - The only type of SMD capacitor suitable for board level active filters is the COG (sometimes called NPO) dielectric type giving the lowest tempco. These are readily available in 1% precisions (at <$0.03/each) but only in E24 steps (5% steps). It also seems they stop being available at low cost above a 12nF maximum value. Other steps, or higher values, are special order and much more expensive.
Key Design Issues in the Low Pass Algorithms

For a multistage filter with overall filter gain > 1,

- How do you allocate the gains between the stages?
- Tightly linked with this question, is, how do you sequence the Q’s in a multistage filter?

With the required K, Q, and Fo in each stage, along with a target maximum final output swing and total supply voltage intended for the design, can we screen then rank the possible op amps that can be applied to each stage?

  - This is looking at supply voltages, slew rates and speed margins required in each stage.

With a target K, Q, Fo and op amp chosen for each stage, can we hit that frequency response (design the R’s and C’s) in a way the improves the resulting noise and distortion in that stage?

  - Can we control the noise added by the resistors?
  - Can we select solutions that limit the internal noise gain peaking?
The idea of an “Optimum” design is illusory

• Really a very multi-dimensional, non-linear, solutions space. All you can really do is go in one direction as far as it makes sense before some other issue rears its ugly head to become a problem.

Nevertheless, current designs delivered from online vendor tools are very far from “optimized”.

• Pretty easy to improve on those with some common sense assumptions.
  − Don’t let the resistors dominate your noise
  − Don’t get constrained by legacy literature for equal R, equal C, and/or K=1
Unique issues to board level active filter designs

Most active filter design literature is headed towards IC implementation.

Our task was to enable successful board level designs using off the shelf (Intersil) op amps.

Discrete implementations have several advantages/disadvantages over IC design flows.

- Active blocks available in discrete steps with unique limitations in each part (output swing, slew rate, noise, bandwidth)
- Not as restrictive on component ratio’ing. R’s and C’s can be chosen a bit more freely with low cost 1% precisions available at low cost.
- Low temp. drift implies COG dielectric. SMD versions readily available in E24 (5% steps) up to 12nF.
Partial List of design considerations in the Low Pass tool

For multi-stage designs, allocate the gains and sequence the Q’s in a way that will enhance dynamic range in the filter implementation

• This led to a descending Q with an ascending gain in each stage that is opposite from most legacy literature and design tools. Have proven that there are significant advantages to this approach.

For each individual stage, consider the stage requirements to screen out parts that will not work and then rank the remaining devices by suitability to the AC and DC requirements of that particular stage.

• These included clipping considerations, BW requirements, slew rate requirements etc. It did not explicitly include noise here – but once an op amp is chosen for a stage, the design scales the R’s to not significantly impact the noise set by the op amp chosen.
Once the target performance and a part is chosen for each stage, execute a design that delivers lower noise and noise peaking inside that stage. This is simply solving for the required R’s and C’s in each stage in a more sophisticated way than normally observed, or reported – for instance:

- Equal R is very common, but does not actually give the sensitivity benefit most authors believe and going to a certain range of R ratios will lower the noise gain peaking.

The solution list of amplifiers assumes some resistor value adjustments to account for amplifier bandwidth to hit the desired filter shape.

- This allows much reduced BW margin in the op amps that can be applied. This yields a much larger range of possible op amps for any particular requirement than most vendor tools.
- This is an algorithm unique to each topology that was tested to hit the target Fo & Q with +/-2% tolerance for a +/-15% BW variation. This set the minimum allowed bandwidth and going up from there in the actual bandwidth chosen reduces this sensitivity.
# Op Amp Model List with New MacroModels

Table of op amps in the Intersil Active Filter Designer – sorted by VFA then CFA and then by ascending GBP or BW (for CFA) as of Dec. 2010

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ISL28194</td>
<td>VFA</td>
<td></td>
<td>0.0035</td>
<td>5</td>
<td>0.00033</td>
<td>1.8</td>
<td>5.5</td>
<td>ISL28194</td>
<td></td>
<td></td>
<td></td>
<td>ISL28194</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28195</td>
<td>VFA</td>
<td>0.01</td>
<td>5</td>
<td>0</td>
<td>0.001</td>
<td>1.8</td>
<td>5.5</td>
<td>ISL28195</td>
<td></td>
<td></td>
<td></td>
<td>ISL28195</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28158</td>
<td>VFA</td>
<td>0.2</td>
<td>5</td>
<td>0</td>
<td>0.034</td>
<td>2.4</td>
<td>5.5</td>
<td>ISL28158</td>
<td>ISL28258</td>
<td></td>
<td></td>
<td>ISL28158</td>
<td>ISL28258</td>
<td></td>
</tr>
<tr>
<td>ISL28156</td>
<td>VFA</td>
<td>0.25</td>
<td>5</td>
<td>0</td>
<td>0.039</td>
<td>2.4</td>
<td>5.5</td>
<td>ISL28156</td>
<td>ISL28256</td>
<td></td>
<td></td>
<td>ISL28156</td>
<td>ISL28256</td>
<td></td>
</tr>
<tr>
<td>ISL28133</td>
<td>VFA</td>
<td>0.4</td>
<td>5</td>
<td>0</td>
<td>0.018</td>
<td>2</td>
<td>5.5</td>
<td>ISL28233</td>
<td>ISL28433</td>
<td></td>
<td></td>
<td>ISL28233</td>
<td>ISL28433</td>
<td></td>
</tr>
<tr>
<td>EL8176</td>
<td>VFA</td>
<td>0.4</td>
<td>5</td>
<td>0</td>
<td>0.055</td>
<td>2.4</td>
<td>5.5</td>
<td>ISL28276</td>
<td>ISL28476</td>
<td></td>
<td></td>
<td>ISL28276</td>
<td>ISL28476</td>
<td></td>
</tr>
<tr>
<td>ISL28107</td>
<td>VFA</td>
<td>1</td>
<td>30</td>
<td>0.21</td>
<td>4.5</td>
<td>40</td>
<td>ISL28207</td>
<td></td>
<td></td>
<td></td>
<td>ISL28207</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28117</td>
<td>VFA</td>
<td>1.5</td>
<td>30</td>
<td>0.44</td>
<td>4.5</td>
<td>40</td>
<td>ISL28217</td>
<td></td>
<td></td>
<td></td>
<td>ISL28217</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28113</td>
<td>VFA</td>
<td>2</td>
<td>5</td>
<td>0.09</td>
<td>1.8</td>
<td>5.5</td>
<td>ISL28213</td>
<td>ISL28413</td>
<td></td>
<td></td>
<td>ISL28213</td>
<td>ISL28413</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28136</td>
<td>VFA</td>
<td>5.1</td>
<td>5</td>
<td>0.9</td>
<td>2.4</td>
<td>5.5</td>
<td>ISL28236</td>
<td>ISL28236</td>
<td></td>
<td></td>
<td>ISL28236</td>
<td>ISL28236</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28114</td>
<td>VFA</td>
<td>7.7</td>
<td>5</td>
<td>0.4</td>
<td>1.8</td>
<td>5.5</td>
<td>ISL28214</td>
<td>ISL28414</td>
<td></td>
<td></td>
<td>ISL28214</td>
<td>ISL28414</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28127</td>
<td>VFA</td>
<td>10</td>
<td>30</td>
<td>2.2</td>
<td>4.5</td>
<td>40</td>
<td>ISL28227</td>
<td></td>
<td></td>
<td></td>
<td>ISL28227</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28110</td>
<td>VFA</td>
<td>12</td>
<td>30</td>
<td>2.6</td>
<td>9</td>
<td>40</td>
<td>ISL28210</td>
<td></td>
<td></td>
<td></td>
<td>ISL28210</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL24021</td>
<td>VFA</td>
<td>15</td>
<td>10</td>
<td>2</td>
<td>4.5</td>
<td>19</td>
<td>ISL28191</td>
<td>ISL28921</td>
<td></td>
<td></td>
<td>ISL28191</td>
<td>ISL28921</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28191</td>
<td>VFA</td>
<td>61</td>
<td>5</td>
<td>2.6</td>
<td>3</td>
<td>5.5</td>
<td>ISL28191</td>
<td>ISL28921</td>
<td></td>
<td></td>
<td>ISL28191</td>
<td>ISL28921</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL55001</td>
<td>VFA</td>
<td>68</td>
<td>30</td>
<td>9</td>
<td>8</td>
<td>30</td>
<td>ISL55002</td>
<td></td>
<td></td>
<td></td>
<td>ISL55002</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL28190</td>
<td>VFA</td>
<td>83.3</td>
<td>5</td>
<td>8.5</td>
<td>3</td>
<td>5.5</td>
<td>ISL28190</td>
<td>ISL28290</td>
<td></td>
<td></td>
<td>ISL28190</td>
<td>ISL28290</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL8101</td>
<td>VFA</td>
<td>106</td>
<td>5</td>
<td>2</td>
<td>3</td>
<td>5.5</td>
<td>EL8100</td>
<td>EL8201</td>
<td>EL8401</td>
<td></td>
<td>EL8100</td>
<td>EL8201</td>
<td>EL8401</td>
<td></td>
</tr>
<tr>
<td>EL5103</td>
<td>VFA</td>
<td>165</td>
<td>10</td>
<td>2.5</td>
<td>5</td>
<td>12.6</td>
<td>EL5102</td>
<td>EL5203</td>
<td></td>
<td></td>
<td>EL5102</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL5101</td>
<td>VFA</td>
<td>170</td>
<td>10</td>
<td>2.5</td>
<td>5</td>
<td>12.6</td>
<td>EL5100</td>
<td></td>
<td></td>
<td></td>
<td>EL5100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL8103</td>
<td>VFA</td>
<td>198</td>
<td>5</td>
<td>5.6</td>
<td>4</td>
<td>5.5</td>
<td>EL8102</td>
<td></td>
<td></td>
<td></td>
<td>EL8102</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL5105</td>
<td>VFA</td>
<td>264</td>
<td>10</td>
<td>5</td>
<td>5</td>
<td>12.6</td>
<td>EL5104</td>
<td>EL5205</td>
<td></td>
<td></td>
<td>EL5104</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2126</td>
<td>VFA</td>
<td>500</td>
<td>30</td>
<td>5</td>
<td>4</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2125</td>
<td>VFA</td>
<td>700</td>
<td>30</td>
<td>10.8</td>
<td>4</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL55190</td>
<td>VFA</td>
<td>700</td>
<td>5</td>
<td>16</td>
<td>3</td>
<td>5.5</td>
<td>ISL55290</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL5131</td>
<td>VFA</td>
<td>900</td>
<td>10</td>
<td>3.5</td>
<td>5</td>
<td>13</td>
<td>EL5130</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL5161</td>
<td>CFA</td>
<td>95</td>
<td>10</td>
<td>0.75</td>
<td>5</td>
<td>12.6</td>
<td>EL5160</td>
<td>EL5261</td>
<td></td>
<td></td>
<td>EL5160</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL5163</td>
<td>CFA</td>
<td>140</td>
<td>10</td>
<td>1.5</td>
<td>5</td>
<td>12.6</td>
<td>EL5162</td>
<td>EL5263</td>
<td></td>
<td></td>
<td>EL5162</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL8108</td>
<td>CFA</td>
<td>190</td>
<td>12</td>
<td>14.3</td>
<td>4.5</td>
<td>13</td>
<td>EL8108</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HFA1105</td>
<td>CFA</td>
<td>270</td>
<td>10</td>
<td>5.8</td>
<td>9</td>
<td>11</td>
<td>HFA1145</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HFA1109</td>
<td>CFA</td>
<td>340</td>
<td>10</td>
<td>9.6</td>
<td>9</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL5165</td>
<td>CFA</td>
<td>370</td>
<td>10</td>
<td>5</td>
<td>5</td>
<td>12.6</td>
<td>EL5164</td>
<td></td>
<td></td>
<td></td>
<td>EL5164</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL5167</td>
<td>CFA</td>
<td>620</td>
<td>10</td>
<td>8.5</td>
<td>5</td>
<td>12.6</td>
<td>EL5166</td>
<td></td>
<td></td>
<td></td>
<td>EL5166</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Typical, room temp., nominal power supply voltages used to produce the following characteristics:

- Open and closed loop I/O impedances
- Open loop gain and phase
- Closed loop bandwidth and frequency response peaking under different external conditions
- Loading effects on closed loop frequency response
- Input noise terms including 1/f effects
- Slew rate
- Input and Output Headroom limits to I/O voltage swing
- Supply current at nominal specified supply voltages
- Nominal input DC error terms (1/3 of specified data sheet test or specified limits – intended to give 1σ error term on one polarity)
- Load current reflected into the power supply current
• Example, single stage design validation. Trying to hit an Fo = 5Mhz, Q = 2.2, gain of 2. Output R was actually 950ohm to get lighter loading.

• Measured response fit the desired shape very closely (once we included the V+ parasitic C in the computations for the R’s)

• But why is it going flat at high frequencies?
Features not supported by the Macromodels

- Harmonic distortion effects
- Composite video differential gain and phase errors
- Output current limiting (if any)
- Disable operation (if any)
- Thermal effects and/or over temperature parameter variation
- Limited performance variation vs. supply voltage modeled
- Part to part performance variation due to normal process parameter spread
- Any performance difference arising from different packaging
- Multichannel device crosstalk effects
Comment on reported speeds

• The Gain Bandwidth Product for the VFA op amps is a critical parameter for the filter designs. The numbers used in the tool may not exactly match what are in the data sheets. Most of the data sheet numbers are more oriented towards gain of 1 and tend to overestimate a true GBP if you need to run at higher gains. The one used in the filter tool will typically underestimate the gain of 1 BW, but get a better fit over a range of gains.

• The BW number is for the CFA amplifiers and represents a number we can hold approximately constant over gains of 1 to X where X is a maximum gain for each part before we have to start increasing the Rf to limit loading effects. It also will appear a bit lower than the data sheet gain of 1 number since it is what we can hit reliably at gains > 1. The maximum gain with constant BW is typically in the 3 ->4V/V region for the current ISL CFA op amps.
**Enhanced Capability Provided by the Tool**

Semi-automatic design flow for multi-stage filters

- Spreads the gain (from 1 to 10V/V total) between the stages and sequences the poles (order >2) in a way that reduces non-linear effects.

Significantly improved circuit implementations.

- Noise effects considered and reduced if possible
- 2nd order issues in the feedback and gain setting elements considered (loading, noise, BW, phase margin)

Resistor solutions adjusted to account for amplifier bandwidth effects to hit the desired pole locations more precisely. This also allows reduced amplifier bandwidth vs. target Fo design margin than any currently available design tool.
Some Common Misconceptions about Active Filters

The Active Filter Designer includes numerous features that might appear to violate some widespread myths –

- Current feedback amplifiers (CFA’s) cannot be used in active filters.
  - They are in fact very suitable as wideband gain blocks (or gain of 1) if that is what is needed in the filter stage. Cannot be used (easily) with reactive feedback type topologies such as the MFB (or infinite gain) circuit.

- Gain of 1 is required for the active filters (or low gain)
  - The gain is a design variable and can be accounted for in setting the R’s and C’s. But it does interact strongly with the amplifier bandwidth if VFA devices are used – and this is also accounted for in the design algorithms here. Also, high gain with high Q should be avoided and is in the semi-automatic flow.

- Equal R or Equal C designs are required or desirable.
  - This comes from simplified academic developments or where the text is headed towards integrated solutions (close cap. ratio’s desirable for integrated filters). Not really a required constraint for discrete implementations and using equal C pushes you into poor designs in some cases.
Technical background for key new elements

• Lot’s of things look different in the delivered designs vs. legacy literature and on line design tools. Extensive testing and analysis has validated all of them to give superior results – for discrete board level designs (most tools and literature are constrained by an IC implementation bias)

• Some of the key differences that strike most designers first are –
  – Higher Q stages first.
  – Sallen Key stages at non-unity gain and/or unequal R values
  – Amplifiers that seem kind of slow for the target Fo and Q.
  – First stages are often set for low gain – doesn’t that hurt noise?
Gain and Q sequencing in the Automatic design

• When a multi-stage design is required with overall gain >1, the design tool will spread the gain out and sequence the Q’s in a built in algorithmic fashion.

• Lot’s of consternation on what it shows here. Let’s explain –
  – As the Q goes up in a stage, the gain should be going down. This is good for bandwidth margin and resulting sensitivity of Q to gain.
  – For cascaded stages with overall gain > 1, the tool decreases the Q in going from input to output, which, given the earlier comment, means the DC gain is normally increasing going input to output. This bothers people.

• Advantages to this –
  – Build up of amplitudes through the stages reduces slew rate and swing requirements (when peaking or overshoot are considered.

• But, doesn’t this produce higher noise ?? Not really.
Low to high gain sequencing example.

- Most designer’s expect to see most of the gain in the early stages of cascaded stage designs. This is legacy from the Friis equation in RF stages and is normally a valid thing to do.
- However, one assumption in the Friis equation is the gain is flat through the band of interest – not exactly true in higher order cascaded filters.
- For example, letting the tool design a 500kHz, 0.25dB Chebyshev, 6th order filter with an overall gain of 10, gives the following solution using the ISL28191.
Example 6th order design

- As you can see, the first stage is the highest Q with a “DC” gain of 1.5, the 2nd is the next lower Q, with a DC gain of 2, and the final is the lowest Q at a gain of 3.33 (total gain of 10).
- The lowest DC gain being first confuses people – one way to think of it is that most of the “gain” really is in the first stage – IF we look in the region around Fo where most of the noise peaking (and integrated noise contribution) will be happening.
- Taking this design apart and plotting the individual frequency responses for each stage on top of each other gives this plot. Blue is the first stage, red 2nd, green last.
Integrated Noise comparisons

- We were actually thinking of this stage sequencing more in terms of the large noise peaks that higher Q stages produced around Fo. Wanted these earlier in the filter chain where we could then roll those off with later, lower Q and Fo stages.

- Here is an example design comparison between a typical strategy shown in a competitive application note targeting a gain of 100, 8th order Butterworth at 100Hz. This first circuit is the typical design approach from that app. note. Note the increasing Q input to output and most of the gain lumped into the first two stages.

<table>
<thead>
<tr>
<th>STAGE 1</th>
<th>STAGE 2</th>
<th>STAGE 3</th>
<th>STAGE 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain: 10 V/V</td>
<td>Gain: 10 V/V</td>
<td>Gain: 1.0 V/V</td>
<td>Gain: 1.0 V/V</td>
</tr>
<tr>
<td>F₀: 100Hz</td>
<td>F₀: 100Hz</td>
<td>F₀: 100Hz</td>
<td>F₀: 100Hz</td>
</tr>
<tr>
<td>Q: 0.51</td>
<td>Q: 0.601</td>
<td>Q: 0.9</td>
<td>Q: 2.56</td>
</tr>
</tbody>
</table>
Integrated Noise comparisons – Intersil design

This is the same filter implemented more in the descending Q, ascending gain approach from input to output. This is almost completely the reverse of what has been previously published but is the strategy encoded in the semi-automatic design provided by the Intersil Active Filter Designer. Here, we see every stage has to provide some gain and that gain is ascending from input to output along with the target Q for each stage descending from input to output.

**TABLE 2. INTERSIL GAIN AND Q SEQUENCING**

<table>
<thead>
<tr>
<th>STAGE 1</th>
<th>STAGE 2</th>
<th>STAGE 3</th>
<th>STAGE 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain: 1.5 V/V</td>
<td>Gain: 2.5 V/V</td>
<td>Gain: 4.0 V/V</td>
<td>Gain: 6.67 V/V</td>
</tr>
<tr>
<td>$F_0$: 100Hz</td>
<td>$F_0$: 100Hz</td>
<td>$F_0$: 100Hz</td>
<td>$F_0$: 100Hz</td>
</tr>
<tr>
<td>Q: 2.56</td>
<td>Q: 0.9</td>
<td>Q: 0.601</td>
<td>Q: 0.51</td>
</tr>
</tbody>
</table>
Assuming the typical approach is intended to improve the noise performance, we should be able to simulate for the output spot noise then integrate that power to compare the designs. Even though there is more gain up front in the typical approach, the high peaking of the noise in the final highest Q stages really hurts the actual noise performance. (This is coming from the following application note.)
This example showed a very large % difference in output noise just due to the filter terms. Caveats –

• While the absolute levels were very low, they become much more meaningful for higher bandwidth filters perhaps using very low power, higher input noise op amps.

• Here, the resistors were being scaled to be a small part of the total output noise and their ratios set to lower noise gain peaking. Most designs deliver much higher valued resistors at equal value swamping out the op amp noise issues. Both of those mistakes can make the integrated noise much worse but is easily fixed using the design flows shown here.

• This noise gain peaking is also compressing the in band loop gain. All other things being equal, that should be hurting distortion. This is another good reason to have the highest Q stage first at lower swings (when the overall filter is delivering gain). Why put that stage last where the maximum output swing is required coincident with the most loop gain loss due to the noise gain peaking that comes with every high Q filter (this applies to both Sallen Key and MFB).

More detailed analysis has actually exposed an extreme noise gain peaking in the Sallen Key 2nd order low pass as the amplifier gain approaches 1 (from a higher level) in Q>1.5 designs. This moved the built in design algorithms to always assign some small gain to the first high Q stage when the overall filter gain is >1.
Added advantages to the Gain and Q sequencing

- In the filter implementations, the Intersil design tool is computing the slew rate, required bandwidth, and overshoot or peaking limitations in each stage.
- Assigning lower gains to higher Q stages solves for a tighter cluster of required amplifier bandwidths in multi-stage filters.
- Sequencing from low gain to high gain in decreasing Q’s also clusters the required slew rates in each stage closer and limits the possibility of interstage clipping in multi-stage filters set up for an overall gain >1.
- Both of these considerations increase the odds that a single op amp part number can be used in all stages with much more modest design margin in its BW and Slew Rate.
- Tools that do not do this, normally deliver designs where the stage requiring the fastest op amp is what is chosen for all stages leading to overdesign in some of them.
Example design showing requirements cluster

• Here, a 3 stage, 6th order design for a 0.5deg equi-ripple filter with a 200kHz cutoff is shown. The first table is the stage requirements as they are split up in the semi-automatic flow of the filter tool. Note the decreasing Q and increasing gain strategy.

• The 2nd table is bit of an extreme re-design where the Q and Fo sequence is the same, but the gains are now high to low – like someone would do thinking they want most of the gain in the input stage for reduced noise. This is done using the manual option of the tool.

<table>
<thead>
<tr>
<th>#1</th>
<th>#2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Stage1</strong></td>
<td><strong>Stage2</strong></td>
</tr>
<tr>
<td>F0: 414.865 kHz  Q: 1.686  Gain: 1.5</td>
<td>F0: 294.014 kHz  Q: 0.893  Gain: 2</td>
</tr>
<tr>
<td>Topology: Sallen Key</td>
<td>Topology: Sallen Key</td>
</tr>
<tr>
<td>Selected OPAMP: ISL28114</td>
<td>Selected OPAMP: ISL28114</td>
</tr>
</tbody>
</table>
Comparison of op amp requirements

• Sitting on each stage inside the design tool, it computes and reports what it thinks each stage needs for a minimum bandwidth and slew rate in that stage for the op amp. Multiplying stage gain by Bandwidth gives GBP for a VFA design.

• The table below summarizes the requirements for the each stage of designs #1 and #2. Remember, both filters hit exactly the same overall shape and gain – this is just looking at internal requirements implied by the gain and Q sequencing strategy.

• Note how much closer the Bandwidth and Slew Rates are in Design #1.

<table>
<thead>
<tr>
<th>Stage</th>
<th>Fo</th>
<th>Q</th>
<th>Design 1 Gain (V/V)</th>
<th>Stage Bandwidth (MHz)</th>
<th>Stage GainBandwidth Product (MHz)</th>
<th>Stage Slew Rate (V/usec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>414kHz</td>
<td>1.686</td>
<td>1.5</td>
<td>4.8</td>
<td>7.2</td>
<td>1.9</td>
</tr>
<tr>
<td>2</td>
<td>294kHz</td>
<td>0.893</td>
<td>2</td>
<td>2.9</td>
<td>5.8</td>
<td>2.3</td>
</tr>
<tr>
<td>3</td>
<td>196kHz</td>
<td>0.551</td>
<td>3.33</td>
<td>2</td>
<td>6.8</td>
<td>3.1</td>
</tr>
<tr>
<td>Total Gain --&gt;</td>
<td>9.99</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Stage</th>
<th>Fo</th>
<th>Q</th>
<th>Design 2 Gain (V/V)</th>
<th>Stage Bandwidth (MHz)</th>
<th>Stage GainBandwidth Product (MHz)</th>
<th>Stage Slew Rate (V/usec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>414kHz</td>
<td>1.686</td>
<td>5</td>
<td>7</td>
<td>35</td>
<td>6.5</td>
</tr>
<tr>
<td>2</td>
<td>294kHz</td>
<td>0.893</td>
<td>2</td>
<td>2.9</td>
<td>5.8</td>
<td>7.5</td>
</tr>
<tr>
<td>3</td>
<td>196kHz</td>
<td>0.551</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>3.1</td>
</tr>
<tr>
<td>Total Gain --&gt;</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
The design tool encodes a built in gain allocation algorithm that balances a number of issues in an attempt to -

- Reduce integrated output noise
- Cluster the op amp requirements closer together – keeps open the option of using the same device without excessive performance margin in any stage.
- Reduce the chance of interstage clipping due to high Q stage overshoot or peaking.

Alternate strategies can be tested using the manual design option. More detail on this gain allocation and Q sequencing can be found in a recently published (online) EDN article.

- “Advanced considerations for gain and Q sequencing in multistage lowpass active filters” by Michael Steffes, Intersil Corp – EDN, October 4, 2010

But now, let’s get into the individual stage design considerations.
Two common 2nd order low pass topologies used,

- Sallen Key non-inverting topology (can use either VFA or CFA op amps)
- Multiple-Feedback (or infinite gain) topology for inverting stages (best to use unity gain stable VFA for these)

Gain = $K_0 = 1 + \frac{R_f}{R_9}$

Sallen Key Topology

Figure 1. MFB Filter Topology
In both topology design flows, the aim was to –
- Reduce the noise contribution of the resistors if possible (limited by loading and available C considerations)
- Reduce the noise gain peaking inside the op amp loop.
- Hit the desired pole locations accounting for amplifier bandwidth effects.

Similar issues in both. The MFB design flow also scales the resistors and adjusts their ratios to achieve lower noise gain peaking. It also sets a lower limit on the input resistor and feedback resistor to avoid loading issues from the prior stage or in the output of the stage being designed.

The MFB design flows are beyond the scope of this discussion, and the Sallen Key will be described here.
Sallen Key Design Flow in the Intersil Filter tool

• With an implementation op amp selected, and the targets set for a particular stage –
  – DC gain (K), Fo, and Q

• Extract the necessary parameters for the op amp, and start stepping towards an R&C solution.
  1. Initial R1 and R2 resolved in two steps.
     • R1 + R2 noise increases input referred V+ noise terms by < 22%
     • R1/R2 set to lower the internal noise gain peaking (and sensitivity of Q to Ko as it turns out). This is in a 0.2 to 0.7 ratio range.
  2. From these, execute an exact solution for C1 and C2 using ideal equations
Sallen Key Design Flow.

3. Snap exact C1 and C2 values to standard E24 values
   - And here there is also a test for either cap >12nF. If so, reset maximum to 12nF, and uses a limit equation to get the other value.

4. With C1 and C2 set, add the op amp’s input parasitic capacitance to C2 then re-solve for exact R1 and R2 including an op amp bandwidth adjustment
   - Often, that adjustment in R values is very small, but it will probably be the case that putting the circuit values into ideal equations will look like they are slightly off.
   - Snap to desired Resistor precision (exact, 0.5%, 1%, 2% supported).
Sallen Key Design Flow – flat band noise calc.

- Assuming the op amp has been selected based on numerous considerations (price, voltage supply, I/O headroom, speed, and input noise voltage issues)
- With op amp noise terms fixed by the device selected, we can bias the R and C designs to not degrade much further from that.
- The equation used is below where $\gamma = 0.2$ to 0.5 range.
- $R_t = R_1 + R_2$

$$R_t \leq \frac{2kT}{i_n^2} \left( \sqrt{1 + \frac{\gamma}{4} \left( \frac{e_n i_n}{kT} \right)^2} - 1 \right)$$
One of the analysis goals was to extract a closed form solution for the low pass SKF noise gain zeroes parametric on the filter design goals and resistor ratio. The noise gain itself is easy to get, re-writing in a way that shows the impact of different design decisions is less trivial.

What came out of this is that $K=1$ is the worst thing you can do for output integrated noise when the target $Q > 1.5$. And that, just going to a gain of 1.2 to 1.5, makes a huge impact on reducing the integrated noise with very modest added design spread due to sensitivity issues.

So, two things just recently came out of this and updated on line.

- Changed the gain allocations in the iSim Active Filter Designer to always try to keep the first, highest $Q$ stage with a little gain – previously used $k=1$ often.
- Really bad to set out to make a single or multi-stage filter with an overall gain of 1.0 if the $Q>2$. Just asking for a little bit of gain helps dynamic range a lot!!! (say at least 1.5 to 2 for a minimum gain of the overall filter gain).
Gain of 1 bias in the SKF design literature

A lot of legacy literature assumes that gain of 1 is the only viable way to make an SKF low pass design. This comes from two issues.

- Lowest Q sensitivity to gain occurs at K=1. This is not because the sensitivity itself is low, but because the gain is very accurate.
- Gain of 1 gives the most bandwidth in a VFA design. However, today, low power VFA and CFA op amps are available at low cost that provide plenty of bandwidth at higher gains.
- And, if you are going to make an adjustment on the components for bandwidth effects (like the Active Filter Designer does) this is less of an issue.

There are two different sensitivity equations for Q to K for the 2\textsuperscript{nd} order SKF seen in the literature – the first is from Budak and the 2\textsuperscript{nd} from Huelsman – surprisingly, it turns out these are equivalent.

Will come back to this interesting sensitivity issue at the end, but for now, let’s see what we can get out of the noise gain equations to derive our $R_1/R_2$ ratio.
Deriving and then manipulating the noise gain zeroes

Like all op amp based active filters, there is also a noise gain expression sitting inside the filter that is pretty tightly, but not completely, tied to the target filter poles. For the Sallen Key 2\textsuperscript{nd} order low pass, that noise gain expression is here.

$$NG = K \frac{s^2 + s \left( \frac{1}{R_2 C_2} + \frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} \right) + \frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s \left( \frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-K_0}{R_2 C_2} \right) + \frac{1}{R_1 R_2 C_1 C_2}}$$

This can be re-written in terms of the filter targets as follows. Note the added degree of freedom in the linear coefficient of the NG zeroes.

$$NG = K \frac{s^2 + s \left( \frac{\omega_0}{Q_p} + \frac{K}{R_2 C_2} \right) + \omega_0^2}{s^2 + s \left( \frac{\omega_0}{Q_p} \right) + \omega_0^2}$$

And then, we can go back to the first expression and extract out a $Q_z$ expression for the complexness of the noise gain zeroes (always < 0.5)

$$Q_z = \frac{1}{\sqrt{\frac{R_1 C_1}{R_2 C_2} + \sqrt{\frac{R_2 C_2}{R_1 C_1} + \frac{R_1 C_2}{R_2 C_1}}}$$
Recognizing the highly peaked noise gain in the SKF

• In going from DC to $F >> F_o$, the noise gain starts at $K$, then increases due to both the desired filter poles (if they are peaking, $Q_p > 0.707$) and also peaks due to the lower noise gain zero. At $F >> F_o$, the noise gain returns to $K$ which, if the amplifier bandwidth is $>> F_o$, will set the amplifier closed loop bandwidth.

• This amplifier bandwidth will set the frequency that the SKF starts to show a loss of stop band rejection due to feedthrough around $C_1$ as the output impedance starts to rise at bandedge for the op amp itself. (recall the earlier plot of measured ISL28191 SKF filter going flat at higher freq.)

• The key thing here, however, is that the noise gain peaks – and can peak a lot if the noise gain zeroes are widely split around $F_o$.

• If we are successful in making the resistor noise low relative to the op amp voltage noise, this noise gain peaking will be what the op amp voltage noise will see for a frequency response to the output and it will dominate.

• Often, this issue has been masked by picking filter R values that dominate the noise.

• Once we fix this issue, this noise gain peaking issue is the next layer down.
Re-writing the Noise gain Qz in ratiometric terms

- The Q_z equation on the earlier slide doesn’t really help us understand what impact different target K and R1/R2 ratio’s might have.
- However, this can all be re-written as ratios where we can start to pull some sense out of this.
  - Alpha is the resistor ratio
    \[ \alpha = \frac{R_1}{R_2} \]
  - Beta is the capacitor ratio
    \[ \beta = \frac{C_1}{C_2} \]

- Now the key thing is to eliminate \( \beta \) if possible by solving for it in terms of the target filter terms and \( \alpha \) – something we are just going to pick.

\[
\sqrt{\frac{C_1}{C_2}} \equiv \sqrt{\beta} = \frac{2Q_p (1+\alpha)}{\sqrt{\alpha} \left(1+\sqrt{1+4Q_p^2 (1+\alpha)(k-1)}\right)}
\]

- This is probably the most useful result here as it shows that once the target filter K, \( Q_p \) and the resistor ratio is set, the cap. ratio is fixed – or vise versa. This is why targeting equal R or equal C gives odd results sometimes as doing that is also really setting the other ratio.
Deriving and then manipulating the noise gain zeroes

• So, going back to the Q\textsubscript{z} equation we now only have the resistor ratio and the target K and Q\textsubscript{p} involved. It is now possible to generate parametric plots of Q\textsubscript{z} on any of those combinations that are simpler since the C ratio is eliminated.

• What we are looking for here, is things that will move the Q\textsubscript{z} closer to 0.5 (repeated real zeroes). If Q\textsubscript{z} is < 0.35, that is starting to indicate a lower real zero in the noise gain that is starting to add appreciable added peaking to the noise gain just due to the choices made in implementation. For Q\textsubscript{z} = 0.35, the zero < Fo adds approximately another 8dB to the noise gain peak over what the desired filter pole peaking is causing.

• Hiding in all of this discussion is the fundamental fact that an infinite range of R and C combinations will give the same filter shape – we are trying to bias those designs towards lower noise gain peaking.
Plotting the $Q_z$ for different gains and alpha

- We can now go back to the $Q_z$ expression in R’s and C’s and write it totally in terms of $\alpha$ and $\beta$ and then use the equation on the earlier slide to get $\beta$ from the target filter $K$, $Q_p$ and $\alpha$ - which makes things a little easier to plot and interpret.
  - Here is that expression

\[
Q_z = \frac{\sqrt{\alpha \beta}}{\alpha \beta + 1 + \alpha}
\]

- The goal here is to keep the noise gain zeroes from getting widely separated, or, in other words, we prefer $Q_z$ approaching 0.5.
- The first question was what impact does the resistor ratio have? Here are couple of target gains and $Q$’s swept on $\alpha$ and computing $Q_z$
As an example of the computed noise gain (in dB) where a specific target SKF filter stage has been set, and the only variable is the resistor ratio used to set the filter shape. Here the total R values was held constant (to minimize noise) and just their ratio varied. This is targeting the first stage of the earlier example #1 design where $K = 1.5$, $F_0 = 414\text{kHz}$, $Q = 1.686$. Note the steady decrease in peak noise gain as $\alpha$ decreases, but also the significant added peaking for $\alpha > 1$. There is diminishing returns again here as $\alpha < 0.4$, but it is definitely worth going from 1 down into that 0.5 region.
Plotting the $Q_z$ for different gains and Target $Q_p$

- This view of the $Q_z$ dependence on $\alpha$ mainly tells us going down in that ratio uniformly increases the $Q_z$, which reduces the noise gain peaking.
- We can also plot the $Q_z$ with a fixed $\alpha$ but swept gains targeting different filter $Q_p$’s. This shows that as the target $Q_p > 1.5$, going to a gain of 1.0 seems to force the noise gain zeroes to be widely separated. Here we just picked $\alpha = 0.5$
- But, just going up slightly in gain from 1 to say 1.2 pulls the zeroes back closer together greatly reducing the noise peaking.
Lessons for the SKF design flow.

- It is uniformly good to move the $R_1/R_2$ ratio $<1$ – which is quite different than is normally seen. Going to $\alpha>1$ is uniformly going in the wrong direction.
- For a stage with target $Q_p > 1.5$, operating at exactly gain of 1 locks you into a highly peaked noise gain due to the zero spreading effect, even with $\alpha < 1$.
- Going up to a gain of 1.2 to 1.5 helps this a lot.
- For multi-stage filters, asking for just a little bit of overall gain, can actually reduce the final output integrated noise significantly over purely gain of 1 stages. This is assuming the resistors have been set low enough to not dominate these noise gain issues.
- Going to $R_1/R_2$ ratio $<1$ and $K>1$ in an SKF stage raises sensitivity concerns for most people (range of filter response spreads as the R and C tolerances are considered).
- It turns out $R_1/R_2$ ratio $<1$ always improves the sensitivity when all terms are considered, and going to gains of 1.2 to 1.5 doesn’t spread things out too much.
Example low cost 1% C0G capacitors.

- A lot of what is different in this design approach is taking advantage of the much improved passives available today. Here is an example search from a distributor web site showing some useful results – These are all 1%, C0G dielectric, SMD Murata caps – Lots of <$0.03 choices here.
Advanced SKF 2nd order low pass Sensitivities

- Most SKF literature solves for the Q sensitivities to the K and R terms and finds that K=1 and R1 = R2 give simple results and stops there.
- Using the relationship between the resistor ratio and the cap ratio shown earlier, we can take these relationships one step further and move beyond these introductory constraints.
- First, the sensitivities for the $\omega_o$ are not very interesting just being $-1/2$ since the $\omega_o$ is just set by the product of all the R’s and C’s. So, this also suggests some absolute precision in those elements is required or the $\omega_o$ is going to be way off.
- The sensitivities for the Q are much more interesting and completely set by ratio’s – which makes sense as the Q is set by ratio’s.
- Remember what these sensitivities are – they are the % change in Q for a small % change in the R’s, C’s, or the gain K.
- So once we have a value for a sensitivity, we have to multiply it by the expected % range on the element then RSS the 5 terms in the Q sensitivity equations (4 passive element varying randomly and the gain).
Sensitivity Equations for the 2nd order SKF Low Pass

- Using the nomenclature shown in this circuit (and letting $K_0 = K$). This is just the one for $K$, there are two others for the $R$’s and $C$’s (at bottom)

$$S_Q^K = Q \left( \sqrt{\frac{R_1 C_1}{R_2 C_2}} + \sqrt{\frac{R_2 C_2}{R_1 C_1}} + \sqrt{\frac{R_1 C_2}{R_2 C_1}} \right) - 1 = QK \sqrt{\frac{R_1 C_1}{R_2 C_2}}$$

- In the case of $K=1$ and
- $R_1=R_2$, this simplifies to

$$S_Q^K = 2Q^2$$

- Which can be a pretty high value, but the $K=1$ is very accurate essentially removing it from the RSS

- The other two sensitivity equations for the $R$ and $C$ terms are -

$$S_{R_1}^Q = -S_{R_2}^Q = -\frac{1}{2} + Q \sqrt{\frac{R_2 C_2}{R_1 C_1}}$$

$$S_{C_1}^Q = -S_{C_2}^Q = -\frac{1}{2} + Q \sqrt{\frac{C_2}{C_1} \left( \sqrt{\frac{R_1}{R_2}} + \sqrt{\frac{R_2}{R_1}} \right)}$$
Sallen Key Sensitivity functions

- Since the $F_o$ always depends on the product of all the R's and C's, it is a given that some absolute precision is needed to hit the $F_o$ (really $\omega_0$).
- However, the Q is a combination of cap ratio’s and gain (if the resistor ratio is chosen to reduce noise gain peaking). Lower gain requires higher cap ratios to hit a Q and vise versa.
- From Huelsman, the sensitivity of Q to K is given by the following equation.

$$S_Q^o = KQ \sqrt{\frac{R_1}{R_2} * \sqrt{\frac{C_1}{C_2}}}$$

- It is pretty obvious from this equation that if you want to hold this under control,
  - As the Q increases, K should decrease in that stage
  - R1<R2 and C1<C2 is desirable to reduce the terms inside the square root.
- Although we were doing it for different reasons, this is exactly what comes out of the filter design tool.
Sallen Key Sensitivity functions

• From the early work to eliminate the cap ratio from the design equations to allow a simpler analysis of the Qz of the noise gain zeroes, we have an expression for the cap ratios in terms of the resistor ratios that can be used to re-write the sensitivities that only includes the resister ratio and the targets for the filter. This makes it easier to sweep parametric curves on gain and $\alpha$ to see what is happening.

$$\alpha \equiv \frac{R_1}{R_2}$$

$$\sqrt{\frac{C_1}{C_2}} = \frac{2Q(\alpha + 1)}{\sqrt{\alpha} \ast (1 + \sqrt{1 + 4Q^2(\alpha + 1)(k - 1)})}$$

• Taking this definition of $\alpha$ and the link between $C_1/C_2$ and $R_1/R_2$ into the sensitivity equation gives a sensitivity parametric on $(R_1/R_2=\alpha)$ that can be swept on K for different target Q’s.

$$S_K^Q = 2KQ^2\left(\frac{\alpha + 1}{1 + \sqrt{1 + 4Q^2 \ast (\alpha + 1) \ast (k - 1)}}\right)$$
Sallen Key Sensitivity functions in terms of $\alpha$

And here are the remaining sensitivities for the R and C terms rewritten in terms of $\alpha$ and the target filter gain and $Q_p$

$$\alpha = \frac{R_1}{R_2}$$

$$S_{R}^{Q_p} = \pm \frac{1}{2} \left( \frac{1 + \sqrt{1 + 4Q_p^2(\alpha + 1)(K - 1)}}{\alpha + 1} - 1 \right)$$

$$S_{C}^{Q_p} = \pm \left( \frac{\sqrt{1 + 4Q_p^2(\alpha + 1)(K - 1)}}{2} \right)$$

These are not necessarily simpler equations, but they do allow us to plot the different sensitivities as either $K$ or $\alpha$ are swept parametric on $Q_p$.

Taking an example for $Q_p = 2.5$ and running these first for $\alpha = 1$ and then $\alpha = 0.5$ over gains from 1 to 2 will show what is happening.
Separate sensitivities and the dB peaking spread

• Here is a sweep from K=1 to K=2 for a target $Q_p=2.5$ with $R1 = R2$ or $\alpha=1$. This is using 1% tolerances on the R’s and C’s to get the % variation on Q for each term then forming the RSS for the 5 error terms and turning that into a total Q variation and then into an expected peak gain variation in dB (at the max. peaking point).

• We can certainly see here that K=1 is the lowest spread, but what is interesting also is the relative value of the terms. K has the most impact, then C, then the R’s. Note also that until the gain is >1.5, the spread in the dB of peaking is <1dB.
Separate sensitivities and the dB peaking spread

- Here is a sweep from $K=1$ to $K=2$ for a target $Q_p = 2.5$ and $\alpha=.5$ which we know should reduce the noise peaking using that lower $R_1/R_2$ ratio.
- Note in particular that the % vs $K$ and the % vs. $C$ curve have tilted down a bit at the cost of the % in $R$ increasing – but it is still the least impact.
- Here, with $R_1 = 0.5R_2$, we actually don’t see the dB peaking spread exceed 1dB until $K > 1.7$. This is one way to see that $\alpha<1$ actually helps sensitivities. While it increases the % vs. $R$, it actually reduces the other two a bit more giving an overall improvement.

![Graph showing % Q spread vs. K and RSS dB peaking spread](image-url)
Cost/Benefit in moving to K>1 in high Q stages.

- Running with K=1 is the lowest Q sensitivity point as the K can be very accurate.
- However, for high Q stages we know this pushes the noise gain zeroes very far apart giving quite a lot of extra noise peaking inside the stage.
- Let’s design the first stage of a 6th order 0.25dB Chebychev low pass filter first at a gain of 1, with equal R, and then at a K=1.2 and $\alpha = .167$. Both of these steps should be reducing the noise gain peaking, while going from a K = 1 to 1.2 should increase the spread in Q (that we are measuring by running Monte Carlo simulations and looking at the spread in gain at the peak) while reducing $\alpha$ should be slightly reducing the spread.
- Here is the first design circuit at a gain of 1 using the ISL28136. Here we are targeting a $Q_p$ of 5.52 with $R1 = R2$ and $F_o = 100$kHz.
Now we can assign a 1% tolerance to all the R’s and C’s and run a frequency response simulation over 1500 cases and plot the spread that peak. The equations predicted a 0.12dB spread and we see about 0.1dB spread.
Now add a little bit of gain and go to $\alpha < 1$.

Here is the same stage target filter using a gain of 1.2 and $\alpha = 0.167$ and then running the same Monte Carlo does show the gain spread at the peak has gone from 0.1dB to 1.17dB. Big step up but still not too bad for a stage that nominally peaks about 16.8dB. Using 1% R and C tolerance is giving +/-0.6dB spread at this design point.
Reduced noise peaking using a bit of gain.

- Running the output spot noise simulation for each circuit option (again in iSim PE – where we can easily get text files of the data to put into Excel) gives the following spot noise plot. Clearly, going up just a bit from gain of 1 has made a big difference in the spot and estimated integrated noise converted to Vpp. This has come at the cost of an increased expected peaking spread from 0.1dB (gain of 1, equal R) to 1.2dB using a gain of 1.2 and $\alpha = 0.15$

- The detailed noise and sensitivity discussion can be found on EN-Genius as –
- Improved Sallen Key Low Pass Designs Exploit Modern Components and Design Tools
  [http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_101810](http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_101810)
• Once we set a filter target, before we actually execute the R & C design, the requirements in each stage are used to constrain and then sort the available op amps for that stage.

• To do this, the required designer inputs are
  – Total supply voltage (assumed to be the same in all stages)
  – Desired maximum output $V_{pp}$ at the final output.

• From these, the tool works backwards from output to input computing the following for each stage.
  – Bandwidth
  – Slew rate
  – Peak output swing
  – Peak input swing.

• Let’s show an example from the tool.
First Step in Getting to a Filter Implementation

• Coming into the tool fresh will give you the first “Requirements” screen set up to a default condition.
The Tool is Mainly an Implementation Aid.

• Many vendor tools provide some filter shape help as an early step in their tools. This is used to arrive at a desired filter order and pole locations to hit a particular “skirt” shape (how fast the cutoff band rolls off). Usually this is specified in terms of stop band attenuation at a certain frequency above the desired passband.

• The Intersil Active Filter Designer assumes you already know the approximate order and/or filter poles you want to implement and mainly works on getting the right part selected and design implemented in a way the will yield a successful board level implementation.
Mainly intended as an Implementation Aid.

- If you need help deciding on the filter shape, try this web site – (free download that has a lot of filter shape design tools – just need to get the pole locations from here, or the shape description, to use in the Intersil Active Filter Designer)

- Filter Wiz PRO

- [http://www.schematica.com/filter_wiz_files/FWPRO.htm](http://www.schematica.com/filter_wiz_files/FWPRO.htm)

- Exact pole locations and advanced features may require you to purchase the full version.
AC Response Preview

- From whatever settings are used in the upper section of the “Requirements” screen, hitting “Update Preview” will generate the ideal Gain, Phase, and Group delay. These are used later to compare to the actual circuit level implementation. Here is the screen after hitting Update Preview.
Two Primary Flows through the Active Filter Designer

1. Semi-Automatic flow is where you want to use some of the pre-loaded filter shapes and let the tool do most of the work for you. This is the default mode and is what is shown on first entering the tool.
   - This flow also decides for you the sequence of poles (order >2) and how to implement the total target gain. It is essentially sequencing from high to low Q stages in low to higher gains in those stages.

2. Manual Pole selection is where you have some specific pole locations you wish to implement and want to enter those directly.
   - This also allows you to select the Frequencies, Gains and Q’s over a wider range than the semi-automatic path.
   - This is all selected in the row that asks “Enter Poles Manually”. This defaults to “No”, but clicking “Yes” changes this screen to accept user entry for each stage. The order setting still sets the number of stages and an odd order (3 or 5) forces the real pole to be the last stage.
Here, the entry screen has been changed by clicking “Yes” on the “Enter Poles Manually?” line and we have changed the gain in each stage to 10 giving an overall filter gain of 100 (10 in each stage is the maximum for 2 stage designs) and manually set the Q’s to get a 4th order Butterworth shape then hit “Update Preview” again. Then hitting the “Continue” key now ->
Setting up the Design

• Hitting “Continue” from the “Requirements” page will go to the “Setup” page where implementation parameters are considered and available for modification. That screen starts out with some default assumptions.

• This is where the real work begins in matching op amps to the desired filter implementations.

• For multi-stage filters, the most important thing to notice on this next screen is which stage is “active” in the setup screen. This is the red color on the Stage # tab. It comes into this step with the last stage as the default “active” stage. This is where the design constraints can be updated. Those also default to the values shown on the next slide, but can be modified.
Setting up the Design

- The main goal for this step is to pick the right op amps for each stage given the topology, filter targets, and constraints.
Setting up the Design

• The 2nd most important thing is that the “Constraints” can only be changed if you sitting on the final stage as the “active” stage. This is mainly related to the final output Vpp target. That can be updated for the last stage, but is then calculated for all previous stages and hence cannot be updated if you are sitting on those earlier stages for amplifier selection purposes.

• While sitting on each “stage” tab, the tool is computing the implied requirements for that stage. These include –
  – Bandwidth if the stage is non-inverting. Since this can be either a VFA or CFA op amp, gain bandwidth is not used in this line. So, taking the required BW number times the gain will give you the required GainBandwidth Product if you want to use a VFA here.
  – If you change the stage to be inverting, only unity gain stable VFA devices can be used and this computation reports the required Gain Bandwidth Product.
Adjustments Available on the Setup stage

• On any given stage, you can change the topology from non-inverting (default) to inverting and that immediately updates the recommended amplifier list at the bottom (this is the only thing that can be changed when you are sitting on earlier stages)

• Sitting on the last stage, you can change the following global constraints –
  – Desired total supply voltage (range here is 1.8V to 40V). This supply voltage is assumed to be the same for all stages.
  – Maximum final stage Output Swing Vpp (limited to be from 10% to 90% of Vs)
  – Linearity Target – either SFDR if frequency domain or Step if step response
    • If SFDR, also asks for maximum expected frequency and desired distortion range
  – Resistor tolerance (exact, 0.5%, 1%, or 2%)
    • This effects the filter accuracy in that exact R solutions will be snapped to available Exx series values probably shifting the nominal filter shape off somewhat. The capacitors are always delivered as E24 step values since this is what you can buy in COG SMD caps. But you can buy those down to 1% accuracy at <$0.03 in volume.
Slew Rate is a critical design value to consider

• Several of these constraints are feeding into the estimated minimum slew rate required reported on each stage.
  – Slew rate is estimated to achieve either an SFDR target or step response without slew limiting. The SFDR constraint is a necessary but not sufficient condition to achieve a certain distortion level – you might still not get the SFDR with a device offering the reported slew rate, but you reduce your chances if the device does not have at least the reported slew rate for that stage.
  – For a step response, the tool is looking at the pole locations of that stage and the desired nominal Vopp or Vstep at the output. It then computes the peak dV/dT to produce that output from an ideal input step and takes 2X that number for a design target. This is very conservative as most stages don’t have an ideal step coming into them.
  – Possible op amps to use in each stage use this Slew Rate calculation to constrain the list to op amps that offer at least 90% of this calculated value.
Picking Suitable Op Amp Solutions

• The goal of this “Setup” page is to pick a suitable op amp that will work in each stage in the design.
  - If possible, the tool will automatically pick the closest fit as you come into this step, but that can be overridden by picking one of the parts listed at the bottom of the screen.

• These are often different devices auto-filled in each stage, but these can often be made the same device with a little effort.

• One of the intents for the gain vs. Q assignments is to cluster the required bandwidths closer together. Most tools have a huge range of amplifier bandwidths required as they don’t to this well.

• Changing the supply voltage will typically show a completely different set of op amps.

• For instance, going to 10V total supply with 6Vpp output will show the following screen. (hit the “Apply” key after you update the supply voltage and output swing fields)
Modifying the Constraints gives new part choices

- More CFA parts shown here as they work above 5V supply.
Picking Suitable Op Amp Solutions

• The part choices are sorted by minimally acceptable to increasing design margin to the requirements. The top device in the table generated for each stage is deemed minimally suitable and is the default part filled into the top boxes. Going down the list gives more design margin.

• Going beyond this step requires a device selection for each stage before the next step (hitting “Design”)

• At any time, you can change a stage to inverting, which then constrains the solution op amps to be unity gain stable VFA since CFA devices cannot (easily) be applied to the those topologies.

• The Setup and design process works in gain “magnitudes” but it does report if the overall filter is inverting or non-inverting.

• You can mix and match topologies and op amp choices freely going stage to stage.
To summarize, the computed minimum requirements for each stage shown on this screen include -
- Bandwidth if the stage is non-inverting, Gain Bandwidth Product if inverting
- Slew rate
- Maximum Vopp including any step overshoot or frequency response peaking
- Maximum input Vipp.

These terms are used to constrain and sort the table of op amp selections to parts that –
- Can operate at the specified total supply voltage
- Will not clip given that supply voltage and output swing (including any peaking or step overshoot effects) considering the output headroom.
- Provides at least 90% of the computed BW and slew rate.
- Will not limit on the input given the supply voltage and input headroom limits.
Executing the Design

• Once we have design targets for each stage and an op amp selected, hitting the “Design” key will go off and compute the R’s and C’s for each stage and come back with a completed design.

• At that point the total specified supply is split into +/- Vs/2 halves and the design is shown as a DC coupled, ground centered, signal swing implementation.

• Hitting “Design” from the previous screen (10V supply, 6V output swing), gives the following active filter design.
Example Design Output Page

- Note the related parts at the bottom and the simulation options at the top – Hitting the AC tab will run an AC simulation
Output of the AC simulation key.

• Clicking on the Filter AC Output opens a waveform viewer where we can add the Ideal Gain, Phase, and Group Delay. Doing that -
Comparison of Actual to Ideal AC Response.

- This viewer also has two cursors that can be moved and a zoom in feature. Here we see very good overall fit for the simulated filter response vs. ideal. We also see the going flat region at high freq.
Design Summary and Saving/Sharing Options

- Going back to the Filter tool (from the waveform viewer) and clicking Design Summary, will give the following screen.
Design Summary and Saving/Sharing Options

• This summarizes the overall targets, the constraints, and the final circuit design.
• Down below on this screen are the BOM the AC, Transient, and/or noise sims that have been done.
• Most importantly, in the upper right are 3 paths to go on from here –
  – Save the design (the little floppy icon). This saves the design locally in your filter tool folder so you open it up and work on it later. Once saved, you can also share the design by emailing it from the “Saved Designs” tab.
  – Download to PDF. This takes the design summary and creates a pdf version that can be saved (and then easily emailed around – great tool for the FAE’s)
  – Download to iSim PE. This ports the schematic into a more general purpose simulator where added operations can be performed. These include MonteCarlo simulations, re-ordering the stages, converting it to a single supply design, etc.
Summary – new very capable implementation tool

• The tool has a lot of capability for re-design and manually setting R and C values as well if you want to force it to other solutions.
• While it will generate simulations within the filter tool, we can also port designs into a free more general purpose simulator “iSim PE” where lots of interesting things can be done.
• This is where we can run Monte Carlo on the different designs to see if equal R or equal C really do have a sensitivity benefit (for instance).
• Turns out gain of 1 is better for sensitivity – but not because the sensitivity is lower at a gain of 1 (in fact it is not in theory), but just that op amps at a gain of 1 hit that gain very-very-very precisely.
• It also turns out that gain of 1 with Q>1.5 gives a much higher noise gain spike in the passband – just going to gain of 1.2 fixes this without much increase on design spread.
• So if you have something you are wondering about in Sallen Key or MFB filters, this tool can let you try it pretty quickly.