

# 7.5V Radiation Hardened Ultra Low Noise, Precision Voltage Reference

## ISL71090SEH75

The [ISL71090SEH75](#) is an ultra low noise, high DC accuracy precision voltage reference with a wide input voltage range from 9.2V to 30V. The ISL71090SEH75 uses the Intersil advanced bipolar technology to achieve  $1.0\mu V_{P-P}$  noise at 0.1Hz with an accuracy over temperature of 0.15%.

The ISL71090SEH75 offers a 7.5V output voltage with  $10\text{ppm}/^\circ\text{C}$  temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld flatpack package.

The ISL71090SEH75 is ideal for high-end instrumentation, data acquisition and applications requiring high DC precision where low noise performance is critical.

## Applications

- RH voltage regulators precision outputs
- Precision voltage sources for data acquisition system for space applications
- Strain and pressure gauge for space applications

## Features

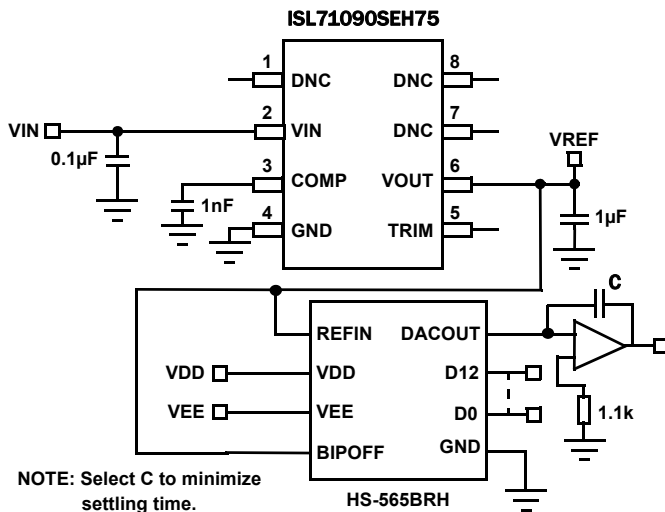
- Reference output voltage .....  $7.5V \pm 0.05\%$
- Accuracy over temperature .....  $\pm 0.15\%$
- Output voltage noise .....  $1.0\mu V_{P-P}$  typ (0.1Hz to 10Hz)
- Supply current .....  $930\mu A$  (typ)
- Tempco (box method) .....  $10\text{ppm}/^\circ\text{C}$  max
- Output current capability ..... 20mA
- Line regulation .....  $8\text{ppm}/V$
- Load regulation .....  $10\text{ppm}/\text{mA}$
- Operating temperature range .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Radiation environment
  - High dose rate (50-300rad(Si)/s) ..... 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) ..... 100krad(Si)\*
  - SET/SEL/SEB .....  $86\text{MeV} \cdot \text{cm}^2/\text{mg}$

\*Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate

- Electrically screened to SMD [5962-13211](#)

## Related Literature

- [AN1847](#), "ISL71090SEH12EV1Z, ISL71090SEH25EV1Z, ISL71090SEH50EV1Z, ISL71090SEH75EV1Z User Guide"
- [AN1848](#), "Single Event Effects (SEE) Testing of the ISL71090SEH Precision Voltage Reference"
- [AN1849](#), "Total Dose Testing of the ISL71090SEH Precision Voltage Reference"



NOTE: Select C to minimize settling time.

FIGURE 1. ISL71090SEH75 TYPICAL APPLICATION DIAGRAM

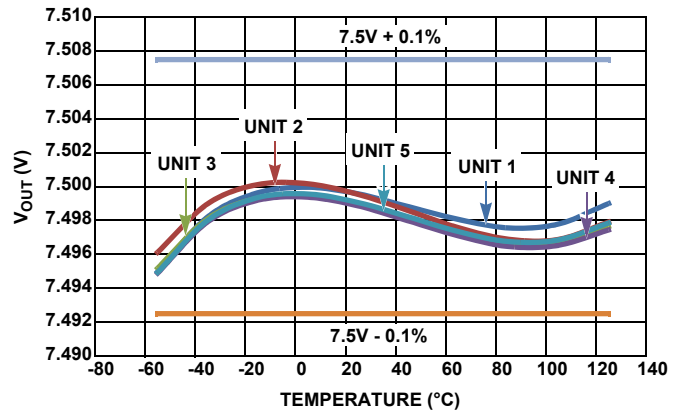


FIGURE 2.  $V_{OUT}$  vs TEMPERATURE

# ISL71090SEH75

## Ordering Information

ORDERING NUMBER (Notes 1, 2)	PART NUMBER	V <sub>OUT</sub> OPTION (V)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R1321104VXC	ISL71090SEHVF75	7.5	-55 to +125	8 Ld Flatpack	K8.A
ISL71090SEHF75/PROTO	ISL71090SEHF75/PROTO	7.5	-55 to +125	8 Ld Flatpack	K8.A
5962R1321104V9A	ISL71090SEHVX75	7.5	-55 to +125	DIE	
ISL71090SEHX75SAMPLE	ISL71090SEHX75SAMPLE	7.5	-55 to +125	DIE	
ISL71090SEH75EV1Z	Evaluation Board				

### NOTES:

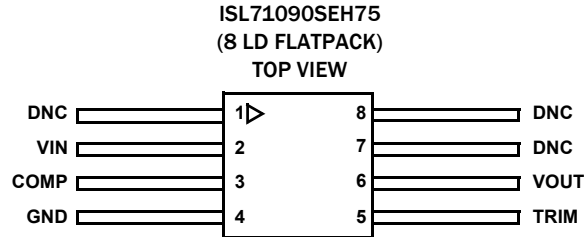
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in this "Ordering Information" table must be used when ordering.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	V <sub>OUT</sub> (V)	TEMPCO (ppm/°C)	OUTPUT VOLTAGE NOISE ( $\mu$ V <sub>P-P</sub> )	LOAD REGULATION (ppm/mA)
ISL71090SEH12	1.25	10	1	35
ISL71090SEH25	2.5	10	2	2.5
ISL71090SEH50	5.0	10	1.1	10
ISL71090SEH75	7.5	10	1	10

# ISL71090SEH75

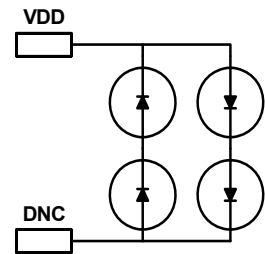
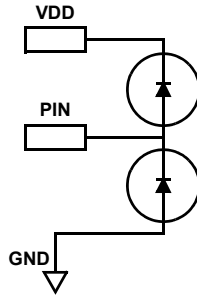
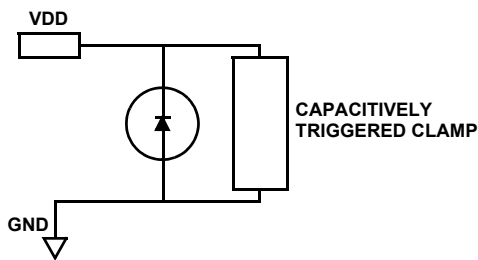
## Pin Configuration



NOTE: The ESD triangular mark is indicative of pin #1. It is a part of the device marking and is placed on the lid in the quadrant where pin #1 is located.

## Pin Descriptions

PIN NUMBER	PIN NAME	ESD CIRCUIT	DESCRIPTION
1, 7, 8	DNC	3	Do not connect. Internally terminated.
2	VIN	1	Input voltage connection
3	COMP	2	Compensation and noise reduction capacitor
4	GND	1	Ground connection. also connected to the lid.
5	TRIM	2	Voltage reference trim input
6	VOUT	2	Voltage reference output



Functional Block Diagram

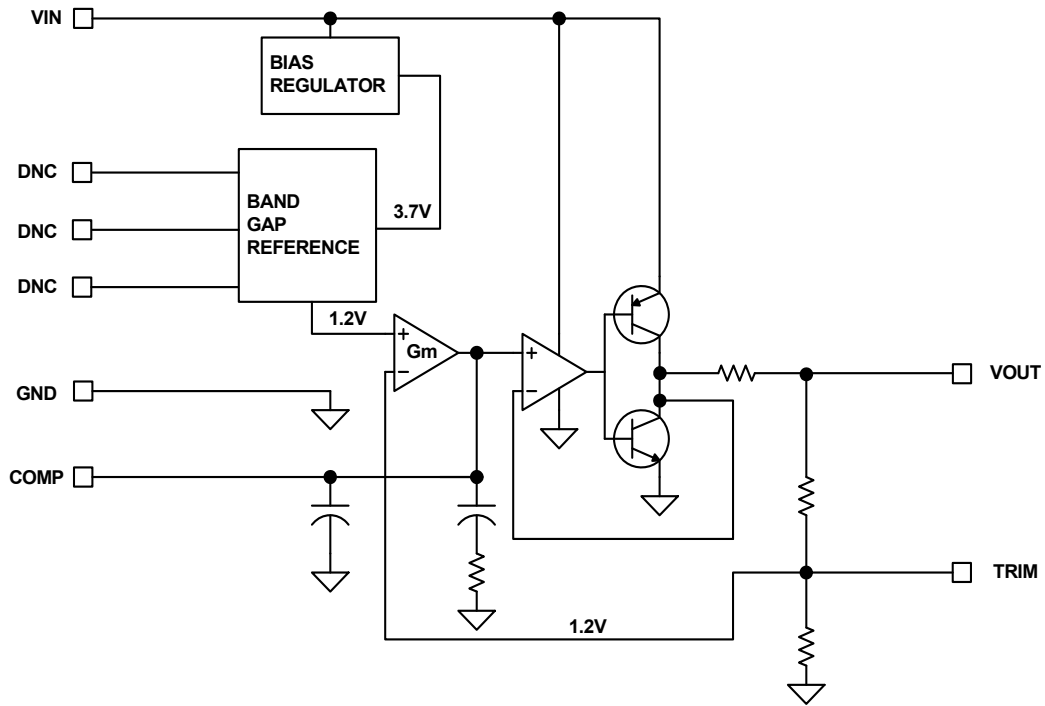


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

# ISL71090SEH75

## Absolute Maximum Ratings

Maximum Voltage	
$V_{IN}$ to GND	-0.5V to +40V
$V_{IN}$ to GND at an LET = 86MeV·cm <sup>2</sup> /mg	-0.5V to +36V
$V_{OUT}$ to GND (10s)	-0.5V to $V_{OUT}$ + 0.5V
Voltage on any Pin to Ground	-0.5V to $V_{OUT}$ + 0.5V
Voltage on DNC Pins	No connections permitted to these pins
ESD Ratings	
Human Body Model (Tested per MIL-PRF-883 3015.7)	2kV
Machine Model (Tested per JESD22-A115-A)	200V
Charged Device Model (Tested per JESD22-C101D)	750V

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
8 Ld Flatpack Package (Notes 3, 4)	140	15
Storage Temperature Range	-65°C to +150°C	
Maximum Junction Temperature ( $T_{JMAX}$ )	+150°C	

## Recommended Operating Conditions

$V_{IN}$	9.2V to +30V
Temperature Range	-55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For  $\theta_{JC}$ , the "case temp" location is the center of the ceramic on the package underside.
- Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.
- The output capacitance used for SEE testing is  $C_{IN} = 0.1\mu\text{F}$  and  $C_{OUT} = 1\mu\text{F}$ .

## Electrical Specifications for Flatpack $V_{IN} = 15\text{V}$ , $I_{OUT} = 0\text{mA}$ , $C_L = 0.1\mu\text{F}$ and $C_C = 1\text{nF}$ unless otherwise specified. **Boldface limits apply after radiation at +25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OUT}$	Output Voltage			7.5		V
$V_{OA}$	$V_{OUT}$ Accuracy at $T_A = +25^\circ\text{C}$	$V_{OUT} = 7.5\text{V}$ , (Note 9)	-0.05		+0.05	%
	$V_{OUT}$ Accuracy at $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$	$V_{OUT} = 7.5\text{V}$ , (Note 9)	<b>-0.15</b>		<b>+0.15</b>	%
	$V_{OUT}$ Accuracy at $T_A = +25^\circ\text{C}$ , Post Radiation	$V_{OUT} = 7.5\text{V}$ , (Note 9)	-0.3		+0.3	%
TC $V_{OUT}$	Output Voltage Temperature Coefficient (Note 8)				<b>10</b>	ppm/°C
$V_{IN}$	Input Voltage Range		<b>9.2</b>		<b>30</b>	V
$I_{IN}$	Supply Current			0.930	<b>1.500</b>	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$V_{IN} = 9.2\text{V}$ to 30V		8	<b>20</b>	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: $0\text{mA} \leq I_{OUT} \leq 20\text{mA}$		10	<b>20</b>	ppm/mA
		Sinking: $-10\text{mA} \leq I_{OUT} \leq 0\text{mA}$		21	<b>40</b>	ppm/mA
$V_D$	Dropout Voltage (Note 10)			1.5	<b>1.7</b>	V
$I_{SC+}$	Short-Circuit Current	$T_A = +25^\circ\text{C}$ , $V_{OUT}$ tied to GND		53		mA
$I_{SC-}$	Short-Circuit Current	$T_A = +25^\circ\text{C}$ , $V_{OUT}$ tied to $V_{IN}$		-63		mA
$t_R$	Turn-On Settling Time	90% of final value, $C_L = 1.0\mu\text{F}$ , $C_C = \text{open}$		250		$\mu\text{s}$
PSRR	Ripple Rejection	$f = 120\text{Hz}$		90		dB
$e_N$	Output Voltage Noise	$0.1\text{Hz} \leq f \leq 10\text{Hz}$		1.0		$\mu\text{V}_{P-P}$
$V_N$	Broadband Voltage Noise	$10\text{Hz} \leq f \leq 1\text{kHz}$		1.2		$\mu\text{V}_{RMS}$
	Noise Density	$f = 1\text{kHz}$ , $V_{IN} = 9.5\text{V}$		38		$\text{nV}/\sqrt{\text{Hz}}$
$\Delta V_{OUT}/\Delta t$	Long Term Drift	$T_A = +125^\circ\text{C}$ , 1000hrs		15		ppm

# ISL71090SEH75

**Electrical Specifications for Die**  $V_{IN} = 15V$ ,  $I_{OUT} = 0mA$ ,  $C_L = 0.1\mu F$  and  $C_C = 1nF$  unless otherwise specified. **Boldface limits apply after radiation at +25 °C and across the operating temperature range, -55 °C to +125 °C without radiation, unless otherwise specified. Specifications over temperature are guaranteed but not production tested on die.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$V_{OUT}$	Output Voltage			7.5		V
$V_{OA}$	$V_{OUT}$ Accuracy at $T_A = +25^\circ C$	$V_{OUT} = 7.5V$ , (Note 11)	-0.05		+0.05	%
	$V_{OUT}$ Accuracy at $T_A = -55^\circ C$ to $+125^\circ C$	$V_{OUT} = 7.5V$ , (Note 11)	<b>-0.15</b>		<b>+0.15</b>	%
	$V_{OUT}$ Accuracy at $T_A = +25^\circ C$ , Post Radiation	$V_{OUT} = 7.5V$ , (Note 11)	-0.3		+0.3	%
TC $V_{OUT}$	Output Voltage Temperature Coefficient (Note 8)				<b>10</b>	ppm/°C
$V_{IN}$	Input Voltage Range		<b>9.2</b>		<b>30</b>	V
$I_{IN}$	Supply Current			0.930	<b>1.500</b>	mA
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation	$V_{IN} = 9.2V$ to $30V$		8	<b>20</b>	ppm/V
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation	Sourcing: $0mA \leq I_{OUT} \leq 20mA$		10	<b>20</b>	ppm/mA
		Sinking: $-10mA \leq I_{OUT} \leq 0mA$		21	<b>40</b>	ppm/mA
$V_D$	Dropout Voltage (Note 10)			1.5	<b>1.7</b>	V

## NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in  $V_{OUT(max)} - V_{OUT(min)}$  is divided by the temperature range; in this case,  $-55^\circ C$  to  $+125^\circ C = +180^\circ C$ .
9. Post-reflow drift for the ISL71090SEH75 devices can be  $100\mu V$  typical based on experimental results with devices on FR4 double sided boards. The engineer must take this into account when considering the reference voltage after assembly.
10. Dropout Voltage is the minimum  $V_{IN} - V_{OUT}$  differential voltage measured at the point where  $V_{OUT}$  drops 1mV from  $V_{IN} = \text{nominal}$  at  $T_A = +25^\circ C$ .
11. The  $V_{OUT}$  accuracy is based on die mount with Silver Glass die attach material such as "QMI 2569" or equivalent in a package with an Alumina ceramic substrate.

## Typical Performance Curves

$V_{OUT} = 7.5V$ ,  $T_A = +25^\circ C$ ,  $C_{OUT} = 1\mu F$ ,  $COMP = 1nF$ , unless otherwise specified.

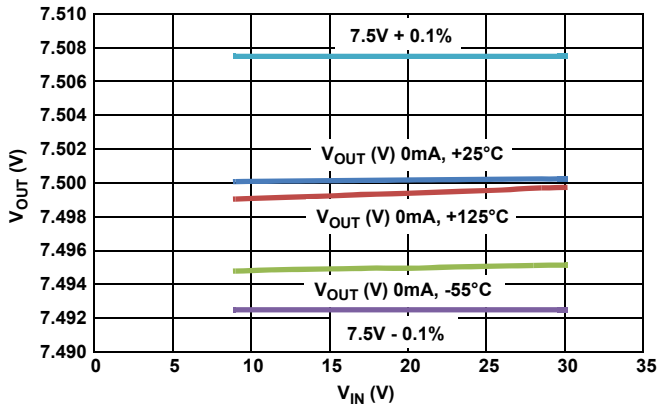


FIGURE 4.  $V_{OUT}$  ACCURACY OVER TEMPERATURE

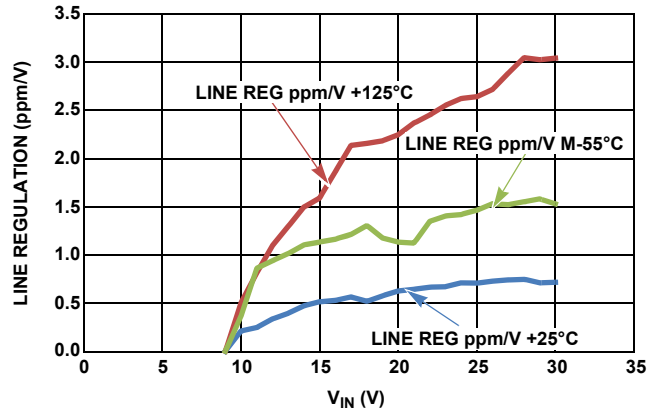


FIGURE 5. LINE REGULATION OVER TEMPERATURE AT  $V_{IN} = 5V$  (ppm/mA)

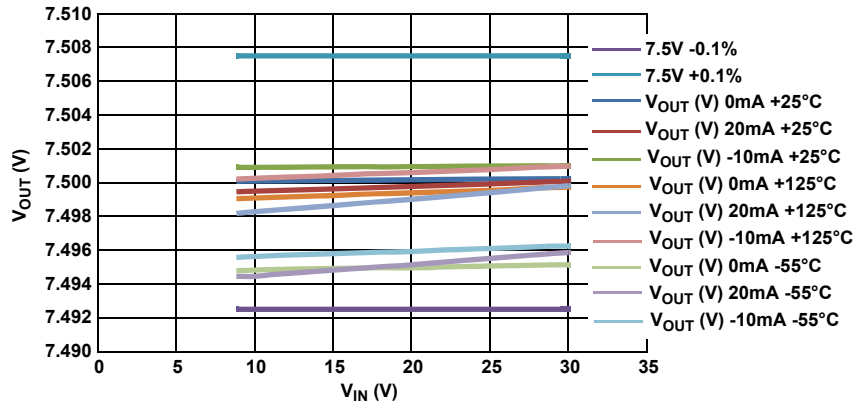


FIGURE 6.  $V_{OUT}$  vs  $V_{IN}$  AT 0mA, 20mA AND -10mA

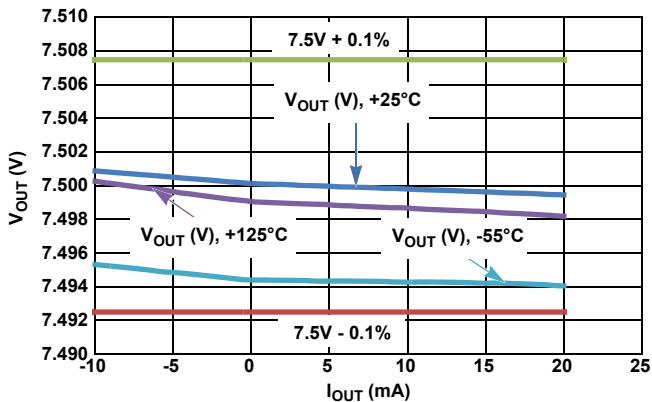


FIGURE 7. LOAD REGULATION OVER TEMPERATURE AT  $V_{IN} = 9.2V$

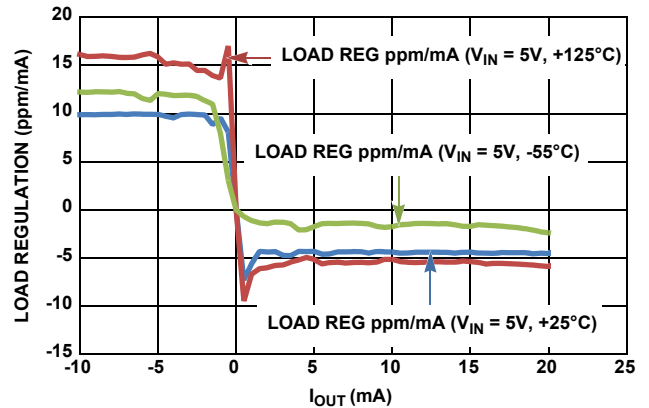


FIGURE 8. LOAD REGULATION OVER TEMPERATURE AT  $V_{IN} = 9.2V$  (ppm/mA)

## Typical Performance Curves $V_{OUT} = 7.5V$ , $T_A = +25^\circ C$ , $C_{OUT} = 1\mu F$ , $COMP = 1nF$ , unless otherwise specified. (Continued)

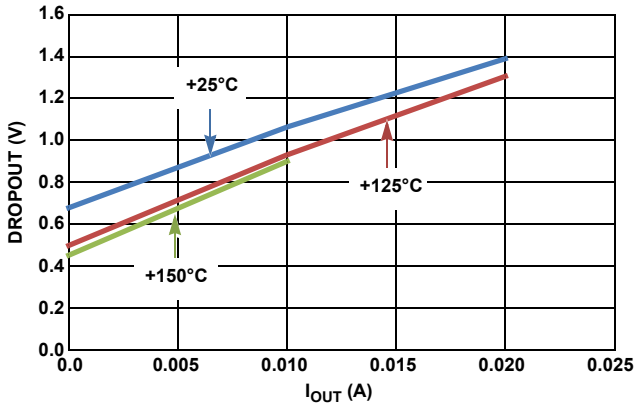


FIGURE 9. DROPOUT VOLTAGE FOR 7.5V

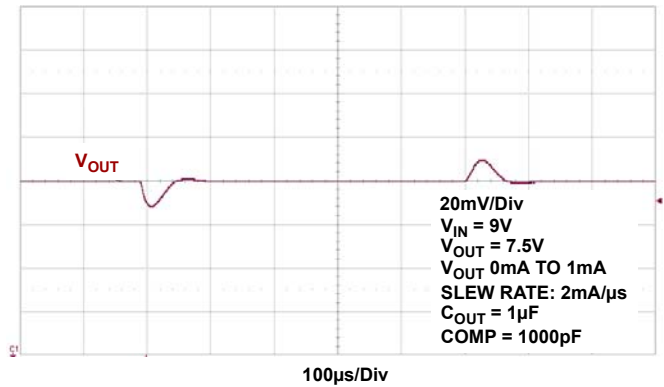


FIGURE 10. LOAD TRANSIENT 0 TO 1mA

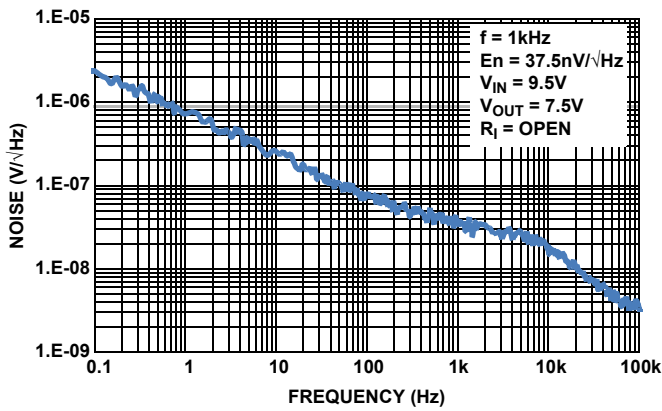


FIGURE 11. NOISE DENSITY vs FREQUENCY ( $V_{IN} = 9.5V$ ,  $V_{OUT} = 7.5V$ ,  $I_{OUT} = 0mA$ )

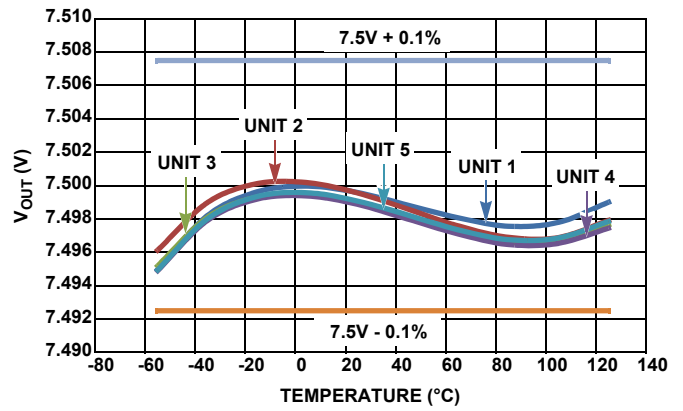


FIGURE 12.  $V_{OUT}$  vs TEMPERATURE

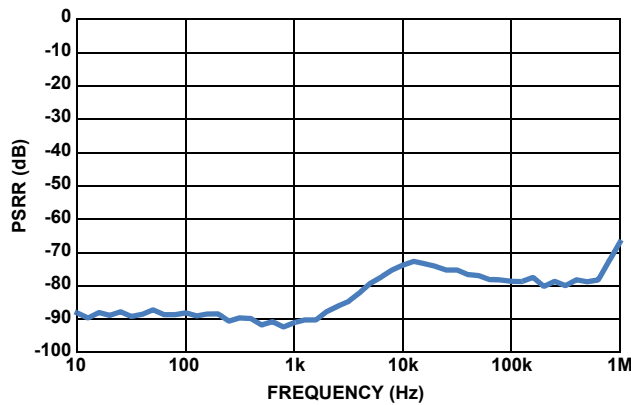


FIGURE 13. PSRR ( $+25^\circ C$ ,  $V_{IN} = 9.5V$ ,  $V_{OUT} = 7.5V$ ,  $I_{OUT} = 0mA$ ,  $C_{IN} = 0.1\mu F$ ,  $C_{OUT} = 1.0\mu F$ ,  $COMP = 1nF$ ,  $V_{SIG} = 300mV_{P-P}$ )



## Device Operation

### Bandgap Precision Reference

The ISL71090SEH75 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive.

## Applications Information

### Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a ceramic flatpack package. Generally, mild stresses to the die when the Printed Circuit (PC) board is heated and cooled, can slightly change the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

### Board Assembly Considerations

Some PC board assembly precautions are necessary. Normal output voltage shifts of typically 100 $\mu$ V can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

### Noise Performance and Reduction

The output noise voltage over the 0.1Hz to 10Hz bandwidth is typically 1.0 $\mu$ V<sub>P-P</sub> ( $V_{OUT} = 7.5V$ ). The noise measurement is made with a 9.9Hz bandpass filter. Noise in the 10Hz to 1kHz bandwidth is approximately 1.2 $\mu$ V<sub>RMS</sub>, with 1 $\mu$ F capacitance on the output. This noise measurement is made with a bandpass filter of 990Hz. Load capacitance up to 10 $\mu$ F (with COMP capacitor listed in [Table 2](#)) can be added but will result in only marginal improvements in output noise and transient response.

### Turn-On Time

Normal turn-on time is typically 250 $\mu$ s, the circuit designer must take this into account when looking at power-up delays or sequencing.

### Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, which provide for the maximum voltage deviation and take the total variation, ( $V_{HIGH} - V_{LOW}$ ), this is then divided by the temperature extremes of measurement ( $T_{HIGH} - T_{LOW}$ ). The result is divided by the nominal reference voltage (at  $T = +25^{\circ}C$ ) and multiplied by  $10^6$  to yield ppm/ $^{\circ}C$ . This is the "Box" method for specifying temperature coefficient.

## Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value via the trim terminal. The trim terminal is the negative feedback divider point of the output op amp. The voltage at the trim pin is set at approximately 1.216V by the internal bandgap and amplifier circuitry of the voltage reference. The suggested method to adjust the output is to connect a 1M $\Omega$  external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a 100k $\Omega$  resistance and whose outer terminals connect to V<sub>OUT</sub> and ground. If a 1M $\Omega$  resistor is connected to trim, the output adjust range will be  $\pm 6.3mV$ . The TRIM pin should not have any capacitor tied to its output, also it is important to minimize the capacitance on the trim terminal during layout to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal to minimize that capacitance and also to minimize noise injection. Small trim adjustments will not disturb the factory-set temperature coefficient of the reference, but trimming near the extreme values can.

## Output Stage

The output stage of the device has a push-pull configuration with an high-side PNP and a low-side NPN. This helps the device to act as a source and sink. The device can source 20mA.

## Use of COMP Capacitor

The reference can be compensated for the C<sub>OUT</sub> capacitors used by adding a capacitor from COMP pin to GND. See [Table 2](#) for recommended values. of the COMP capacitor.

TABLE 2.

C <sub>OUT</sub> ( $\mu$ F)	C <sub>COMP</sub> (nF)
0.1	1
1	1
10	10

## SEE Testing

The SET result is based on the ISL71090SEH25. The ISL71090SEH25 and ISL71090SEH75 share the same active circuitry consisting of a precision bandgap circuit and a trimmable amplifier to set the output reference with only a resistor change to scale the output. The SET test was done under an ion beam having an LET of 86MeV  $\cdot$  cm<sup>2</sup>/mg. The device did not latch up or burn out to a V<sub>DD</sub> of 36V and at +125 $^{\circ}C$ . Single Event transients were observed and are summarized in the [Table 3](#):

TABLE 3.

V <sub>IN</sub> (V)	I <sub>OUT</sub> (mA)	C <sub>OUT</sub> ( $\mu$ F)	SET (% V <sub>OUT</sub> )
4	5	1	-4.6
30	5	1	-4.4
30	5	10	-1.0

## DNC Pins

These pins are for trimming purposes and for factory use only. Do not connect these to the circuit in any way. It will adversely effect the performance of the reference.

# ISL71090SEH75

## Package Characteristics

### Weight of Packaged Device

0.31 Grams (Typical)

### Lid Characteristics

Finish: Gold

Potential: Connected to lead #4 (GND)

Case Isolation to Any Lead:  $20 \times 10^9 \Omega$  (min)

## Die Characteristics

### Die Dimensions

$1464\mu\text{m} \times 1744\mu\text{m}$  (58 mils x 69 mils)

Thickness:  $483\mu\text{m} \pm 25\mu\text{m}$  (19 mils  $\pm$  1 mil)

### Interface Materials

#### GLASSIVATION

Type: Nitrox

Thickness:  $15\text{k}\text{\AA}$

### TOP METALLIZATION

Type: AlCu (99.5%/0.5%)

Thickness:  $30\text{k}\text{\AA}$

### BACKSIDE FINISH

Silicon

## ASSEMBLY RELATED INFORMATION

### SUBSTRATE POTENTIAL

Floating

## ADDITIONAL INFORMATION

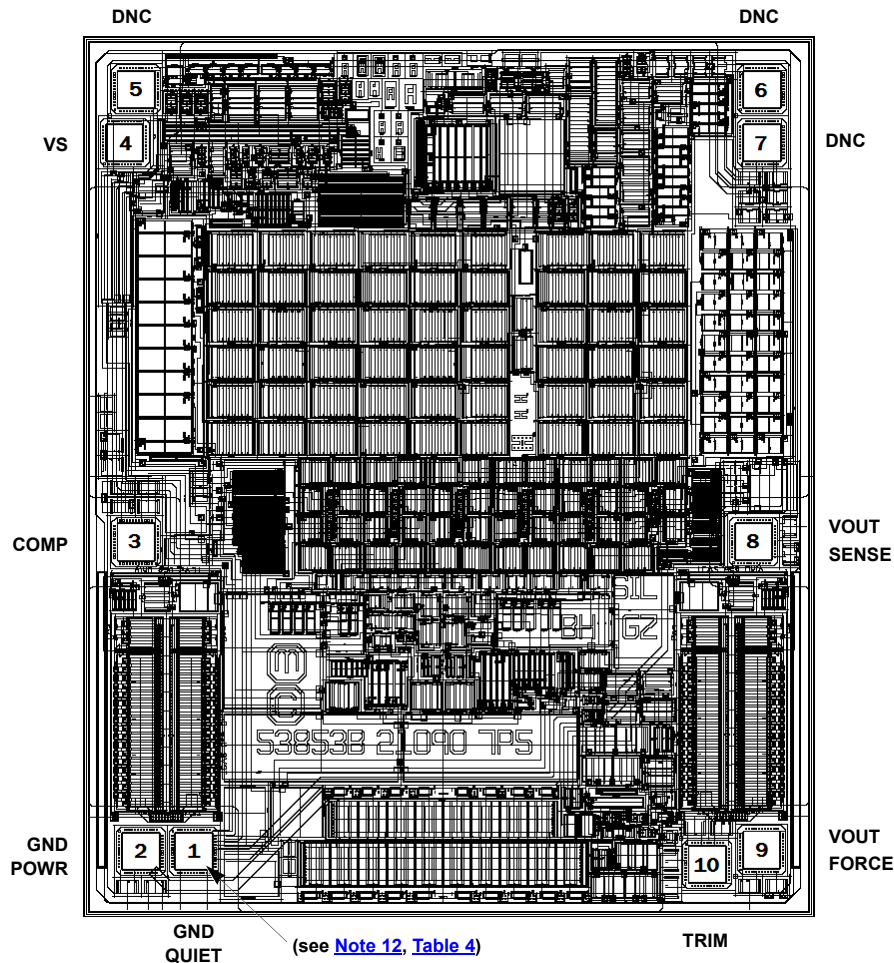
### WORST CASE CURRENT DENSITY

$< 2 \times 10^5 \text{ A/cm}^2$

### PROCESS

Dielectrically Isolated Advanced Bipolar Technology- PR40 SOI

## Metallization Mask Layout



# ISL71090SEH75

TABLE 4. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X ( $\mu\text{m}$ )	Y ( $\mu\text{m}$ )	BOND WIRES PER PAD
GND PWR	2	-104	0	1
GND QUIET	1	0	0	1
COMP	3	-108	589	1
VS	4	-125	1350	1
DNC	5	-108	1452	1
DNC	6	1089	1452	1
DNC	7	1089	1350	1
VOUT SENSE	8	1072	598	1
VOUT FORCE	9	1088	1	1
TRIM	10	985	-25	1

NOTES:

- Origin of coordinates is the centroid of GND QUIET.
- Bond wire size is 1.0 mil.

# ISL71090SEH75

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
March 18, 2016	FN8591.3	<ul style="list-style-type: none"><li>-Changed title from "Radiation Hardened Ultra Low Noise, Precision Voltage Reference" to "7.5V Radiation Hardened Ultra Low Noise, Precision Voltage Reference"</li><li>-Updated Related Literature document titles to match titles on the actual documents.</li><li>-Added Table 1 to page 2.</li><li>-Corrected the Evaluation board part number in the Ordering Information table on page 2.</li><li>-On page 5:<ul style="list-style-type: none"><li>-Changed Electrical Specification for Flatpack note from: "Boldface limits apply over the operating temperature range, -55 °C to +125 °C and radiation." to: "Boldface limits apply after radiation at +25 °C or across the operating temperature range, -55 °C to +125 °C without radiation, unless otherwise specified.</li><li>-For parameter VOA (row 4) in Electrical Specifications for Flatpack table changed description from: "VOUT Accuracy, Post Rad", to: "VOUT Accuracy at TA = +25 °C, Post radiation" and for parameters VOA (rows 2, 3, 4) added "Note 9" to Conditions column.</li></ul></li><li>-On page 6:<ul style="list-style-type: none"><li>-Changed Electrical Specification for Die note from: "Boldface limits apply over the operating temperature range, -55 °C to +125 °C and radiation." To: "Boldface limits apply after radiation at +25 °C or across the operating temperature range, -55 °C to +125 °C without radiation, unless otherwise specified.</li><li>-For parameter VOA (row 4) in Electrical Specifications for Die table changed description from: "VOUT Accuracy, Post Rad", to: "VOUT Accuracy at TA = +25 °C, Post radiation" and for parameters VOA for Post radiation (row 4) added "Note 11" to Conditions column.</li></ul></li><li>-Updated POD K8.A to the latest revision changes are as follows:<ul style="list-style-type: none"><li>Modified Note 2 by adding the words "...in addition to or instead of..."</li></ul></li></ul>
December 2, 2013	FN8591.2	Electrical spec table on page 5 (Flatpack) and page 6 (Die): V <sub>OUT</sub> Accuracy Post Rad section, changed the value for Min from -0.25% to -0.3% and Max from +0.25% to +0.3%.
October 4, 2013	FN8591.1	Initial Release.

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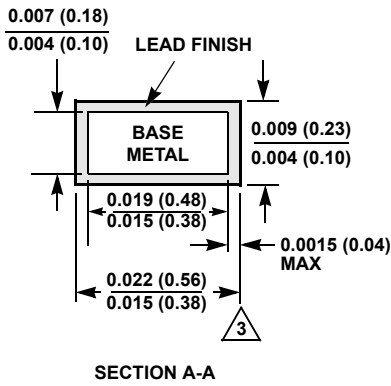
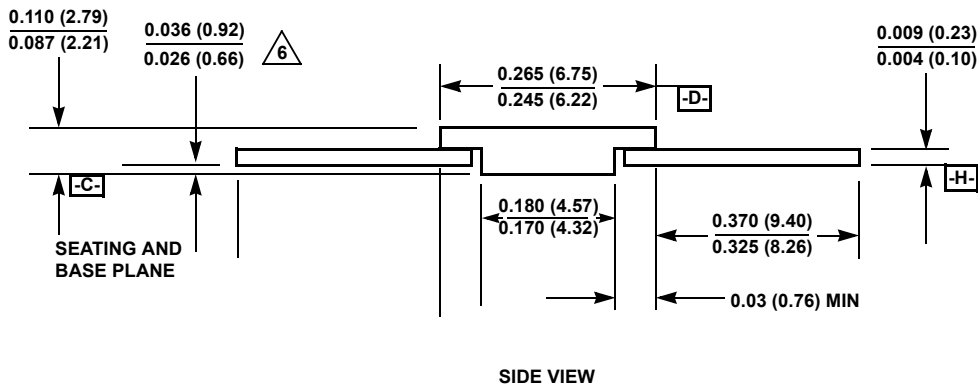
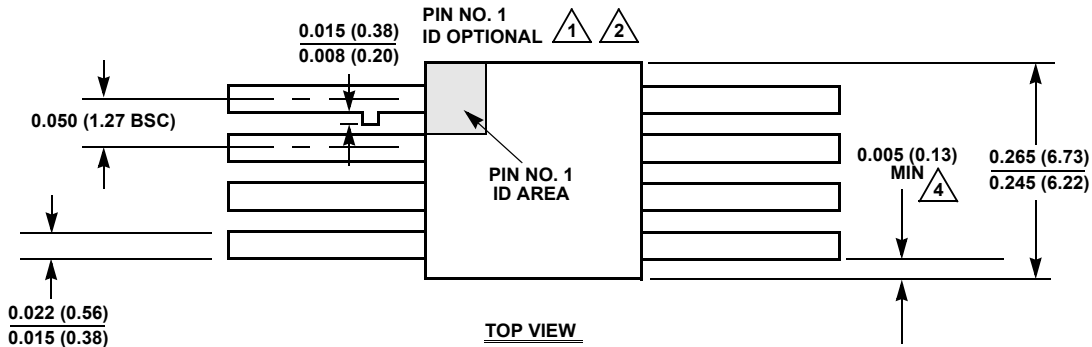
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## Package Outline Drawing

### K8.A

8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 4, 12/14



#### NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.