Introduction

The following text describes the basic test procedures that can be used for most Intersil Op Amps. Note that all measurement conversions have been taken into account in the equations stated.

1. Offset Voltage

The offset voltage ($V_{IO}$) of the amplifier under test (AUT) is measured via Test Circuit 1 as follows:

1. Set $V_+$ and $V_-$ supplies to values specified in Table 1, Column (1) and $V_{DC}$ to 0V.
2. Close S1 and S2, open S3.
4. Measure voltage at E in volts (label as $E_1$).

$$V_{IO} = E_1 \times 10^4 \mu V$$

The gain of this circuit with $R_F = 50K$ ($R_F = 5M$) requires the output to be driven to 1000 (100,000) times the offset voltage necessary to maintain the output of the AUT at 0V. Note that the AUT output is always identical to $V_{DC}$. Overall circuit stability is maintained by the adjustable feedback capacitor $C_A$.

2. Input Bias Current

The bias current flowing in or out of the positive terminal of the AUT ($I_{B+}$) is obtained using Test Circuit 1 by:

1. Measuring $E_1$ as in procedure 1 (use $R_S = 100K$ for JFET input devices).
2. Maintain $V_{DC}$ at 0V.
3. Close S2, open S1 and S3.
4. Measuring voltage at E in volts (label as $E_2$).

$$I_{B+} = \frac{E_1 - E_2}{10^4} \text{nA}$$

The bias current flowing in or out of the negative terminal ($I_{B-}$) is found by:

1. Following steps 1 and 2 for $I_{B+}$.
2. Close S1, open S2 and S3.
3. Measuring voltage at E in volts (label as $E_3$).

$$I_{B-} = \frac{E_1 - E_3}{10^4} \text{nA}$$

4. Power Supply Rejection Ratio

Both positive and negative PSRRs are measured via Test Circuit 1. For PSRR+:

1. Close S1 and S2, open S3.
2. Choose: $R_F = 50K$
3. Set $V_{DC} = 0$, $V_+ = 10V$, and $V_- = -15V$.
4. Measure voltage at E in volts (label as $E_5$).
5. Change $V_+$ to +20V.
6. Measure voltage at E in volts (label as $E_6$).

$$PSRR_+ = 20 \log_{10} \left( \frac{10^4}{E_5 - E_6} \right) \text{dB}$$

Similarly for PSRR-:

1. Follow steps 1 and 2 for PSRR+ above.
2. Set $V_{DC} = 0V$, $V_+ = +15V$, and $V_- = -10$.
3. Measure voltage at E in volts (label as $E_7$).
4. Change $V_-$ to -20V.
5. Measure voltage at E in volts (label as $E_8$).

$$PSRR_- = 20 \log_{10} \left( \frac{10^4}{E_7 - E_8} \right) \text{dB}$$

5. Common Mode Rejection Ratio

The CMRR is determined by adjusting Test Circuit 1 as follows:

1. Close S1 and S2, open S3.
2. Choose: $R_F = 50K$
3. Set $V_+ = +5V$, $V_- = -25V$, and $V_{DC} = -10V$.
4. Measure voltage at E in volts (label as $E_9$).
5. Set $V_+ = 25V$, $V_- = -5V$, and $V_{DC} = 10V$.
6. Measure voltage at E in volts (label as $E_{10}$).

$$CMRR = 20 \log_{10} \left( \frac{2 \times 10^4}{E_9 - E_{10}} \right) \text{dB}$$

6. Output Voltage Swing

Test Circuit 2 is adjusted to measure $V_{OUT+}$ and $V_{OUT-}$ the procedure is:

1. Select appropriate $V_+$ and $V_-$ supply values from Table 1, Column 1.
2. Select specified R_L from Table 1, Column 2.
3. Set V_IN = 0.5V.
4. Measure voltage at E in volts. V_OUT+ = E (V)

Similarly V_OUT+ is found by:
1. Selecting specified R_L from Table 1, Column 1.
2. Setting V_IN = -0.5V.
   \[ V_OUT+ = E (V) \]

7. Output Current

The output current corresponding to the output voltage of procedure 6 is found by:
   \[ I_{OUT+} = \frac{V_{OUT+}}{R_L} \text{ where } R_L \text{ is from Table 1, Column 2.} \]
   \[ I_{OUT-} = \frac{V_{OUT-}}{R_L} \text{ where } R_L \text{ is from Table 1, Column 2.} \]

8. Open Loop Gain

Both positive (AVOL+) and negative (AVOL-) open loop gain measurements are determined by adjusting Test Circuit 1.

For AVOL+:
1. Close S1, S2 and S3.
2. Select specified R_L from Table 1, Column 3.
3. Set R_F = 50K.
4. Set V_DC = 0V, V+ = +15V, and V- = -15V.
5. Measure voltage at E in volts (label as E13).
6. Set V_DC = 10V.
7. Measure voltage at E in volts (label as E14).
   \[ AVOL+ = \frac{10}{E_{14} - E_{13}} (V/mV) \text{ for } R_F = 50K \]

For AVOL-:
1. Follow steps 1, 2, 3, 4, and 5 above.
2. Set V_DC = -10V.
3. Measure voltage at E in volts (label as E15).
   \[ AVOL- = \frac{10}{E_{13} - E_{15}} (V/mV) \text{ for } R_F = 50K \]

9. Slew Rate

Test Circuit 3 is used for measurement of positive and negative slew rate. For SR+:
1. Select specified R_L, A_CL, and C_L from Table 1, Columns 4, 5 and 6.
2. Apply a positive step voltage to V_AC (refer to data book for test waveform).
3. Observe \( \Delta V \) and \( \Delta t \) at E. A standard approach is to use the 10% and 90% points or else the 25% and 75% points on the waveform.

\[ SR = \frac{\Delta V}{\Delta t} \]

For SR- repeat above procedure with negative input pulse.
\[ SR^- = \frac{\Delta V}{\Delta t} \]

10. Full Power Bandwidth

Full power bandwidth is calculated by:
1. Measuring slew rate as above in procedure 9.
2. Measuring V_OUT+ as in procedure 6. (Typically V_OUT+ is assumed to be the guaranteed minimum V_OUT, usually 10V.)
   \[ FPBW = \frac{SR+}{2\pi V_{OUT(PEAK)}} \]

11. Rise Time, Fall Time and Overshoot

The small signal step response of the AUT is determined via Test Circuit 3. The procedure requires:
1. Selecting the appropriate R_L, A_CL, and C_L from Table 1, Columns 4, 5 and 6.
2. Applying a positive input step voltage for rise time t_R and positive overshoot OS+.
   Applying a negative input step voltage for fall time t_F and negative overshoot OS-.
   (Refer to data book for input waveforms.)
3. Observe output of AUT noting the key points as shown.
12. Settling Time

Test Circuit 6 is appropriate for settling time (t_S) measurement, the procedure is:

1. Select R_1 and R_2 such that AUT is at the A_CL stated in Table 1, Column 5.
2. Select R_3 and R_4 so that R_3 ≥ 2R_1 and R_4 ≥ 2R_2 with the condition that the ratio
   \[ \frac{R_3}{R_1} = \frac{R_4}{R_2} \]
   be maintained.
3. Apply step voltage as specified in data book.
4. Measure the time from t_1 (time input step applied) to t_2 (the time E_S settles to within a specified percentage of V_OUT - see data book). t_S = t_2 - t_1

NOTE: Clipping diodes of Test Circuit 6 prevent overdrive of oscilloscope. (Recommend fast Schottky diodes.)

13. Gain Bandwidth Product

Test Circuit 4 is used for measuring GBP. The procedure is:

1. Sweep V_IN thru the required frequency range.
2. With a network analyzer view gain (dB) versus frequency as below.

   ![Gain Bandwidth Product Diagram]

3. At the voltage gain of interest (A_V) determine the corresponding frequency f_C. Note that chosen A_V must be greater than or equal to that stated in column 5 of Table 1. GBP = A_V x f_C (Hz) where A_V is in V/V.

14. Phase Margin (Network Analyzer Method)

Test Circuit 4 is used to obtain phase margin measurement. The procedure is:

1. Sweep V_IN thru the required frequency range.
2. Display gain in dB and phase in degrees versus frequency on analyzer as shown.

3. At a gain of 0dB (if A_CL = 1 in Table 1, column 5), record frequency f_1 and corresponding phase P_1. Phase margin = 180 degrees - P_1 degrees.

15. Input Noise Voltage

Test Circuit 5 is designed for measuring input noise voltage. Use of the Quantec Noise Analyzer is recommended to obtain measurements at 1Hz bandwidth around a specific center frequency. The procedure is:

1. Set R_G = 0
2. Set circuit card to gain of 10.
3. Select measurement frequency of interest.
4. Record noise voltage (label as E_n1). Units are nV/√Hz.

16. Input Noise Current

Using Test Circuit 5, the input noise current is obtained by:

1. Measure E_n1 as above for the desired frequency of interest.
2. Adjust R_G so that V_O > 2E_n1 (label V_O as E_n2).

   \[ I_n = \sqrt{\frac{(E_{n2})^2 - (E_{n1})^2 - 4kTR_G}{R_G^2}} \]

   Where K = 1.38 x 10^{-23} (Boltzmann's Constant)
   T = 300 K (27°C)

17. Channel Separation (Crosstalk)

Test Circuit 7 is used to measure channel separation (CS). The procedure is as follows:

1. Apply V_IN at the frequency of interest to input of channel 1.
2. Select R_L from Table 1, column 4.
4. Measure V_O2 of channel 2.

   \[ CS = 20 \log_{10} \left| \frac{V_{O2}}{100V_{O1}} \right| \text{dB} \]
### TABLE 1.

<table>
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<th>PART NUMBER</th>
<th>(1) SUPPLY VOLTAGE ($V_S$)</th>
<th>(2) $V_{OUT}$ $R_L$(kΩ)</th>
<th>(3) $A_{VOL}$ $R_L$(kΩ)</th>
<th>SLEW RATE, OS, $I_R$, $I_F$</th>
<th>(4) $R_L$(kΩ)</th>
<th>(5) $A_{CL}$</th>
<th>(6) $C_L$(pF)</th>
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Test Circuits

TEST CIRCUIT 1

TEST CIRCUIT 2

TEST CIRCUIT 3

TEST CIRCUIT 4

TEST CIRCUIT 5
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